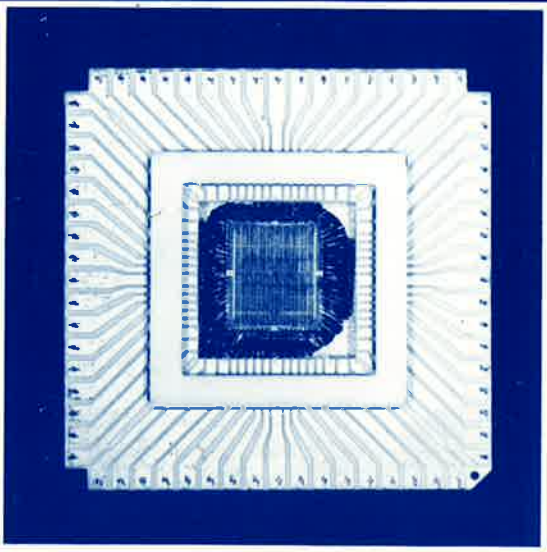
VAX-11/VENUS



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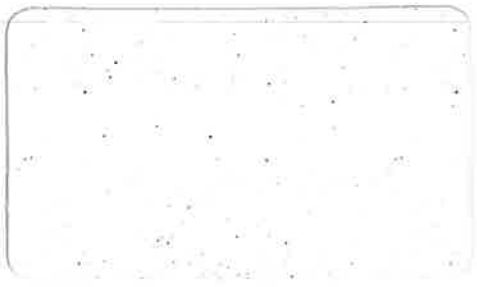

John DeRosa

VENUS

SYSTEM
DEVELOPMENT PLAN

16 September 1982
Revision 4

C O M P A N Y C O N F I D E N T I A L

C O M P A N Y C O N F I D E N T I A L

This document contains confidential information on new products that should be disclosed only to those people engaged in the Program. Under no circumstances should any non-DEC persons be informed about any aspects of the Program or its existence.

Issued by Sultan Zia

Edited by Bill English and Barbara Watterson

16 September 1982
Revision 4


digital
VENUS LARGE CI SYSTEM

VENUS SYSTEM DEVELOPMENT PLAN

This plan presents a description of the proposed course of the VENUS Program. The first section is an executive summary that touches on the essentials of the plan. The next four sections explain what the system is, how it will be developed, how much it will cost, and how the objective of the development program - a marketable system - will be realized. The final section gives more detailed information about the functionality of the various parts of the system.

All of the information given in this plan is necessarily summary in nature, and is derived from the much more detailed plans and specifications for the individual parts of the Program. Appendix A itemizes the capital equipment to be included in the Engineering prototypes. Appendix B lists the product requirements as defined by the Product Lines in conjunction with Product Management and also gives Engineering's response to these requirements. Appendix C identifies all of the people associated with the Program. This is followed by a Glossary of some of the terms and acronyms used in this document.

The fundamental objective of the VENUS Program is to bring a competitive system to market as soon as possible. With this in mind, we are developing an initial system based on the traditional Unibus for communications and unit record, and the new CI-HSC for mass storage. A system based on the CI project and its peripherals is expected to be delivered within the VENUS timeframe. As soon as the initial system is complete, the VENUS design team will begin work on a mid-life kicker, involving conversion to NI and implementation of advanced packaging.

This plan has been approved by the VENUS managers and supervisors whose signatures appear on the next page.

By signing this plan each of us indicates, in our best judgment, that

1) I understand this plan and feel that I fully appreciate its implications both for myself and for the VENUS Program;

2) I am aware of the expectations the VENUS Program has of my group, and I am confident we can fulfill those expectations;

3) This plan fully addresses all expectations I have of the VENUS Program, and I feel confident the Program can fulfill those expectations;

4) I am confident that, overall, the objectives of this plan are achievable in the timeframe indicated; and

5) I will communicate, in writing, to the Program Manager any specific reservations that I have about any item in the plan.

System Development Manager
Bob Glorioso

Program Manager
Sultan Zia

Product Manager
Carl Gibson

Technology Project
Vic Ku

CPU Project
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CPU Engineering
Alan Kotok

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Carl Gibson

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Qualification Engineering
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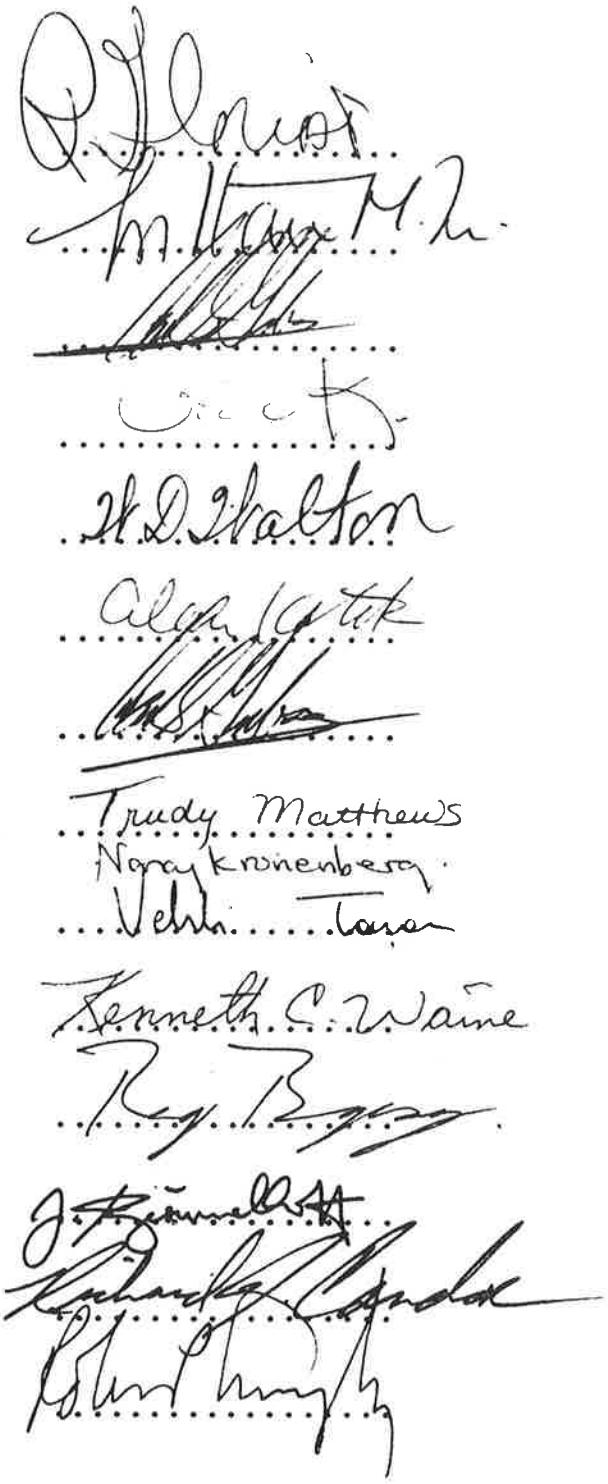

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Glossary

1 THE VENUS PROGRAM

This section summarizes the elements of the Program. Here and elsewhere in this plan, the discussion of schedules and commitments employs such terms as FRS and FVC; these terms are explained in the Glossary.

1.1 PROGRAM PRIORITIES AND HIGHLIGHTS

At the core of the Program is an engineering development plan organized around a set of priorities or overall goals. Within the framework of these goals, we have defined a product using state-of-the-art technology.

Program Priorities

The development strategy is geared to these goals listed in order of importance to the Program.

FRS by 6/84; total number of systems shipped in first two years: 45 in FY84, 1,392 in FY85

Maximize customer satisfaction (superior to comparable IBM systems)

Maximize life cycle profit

Cost of ownership less than comparable 11/780 systems

Meet transfer cost targets: comparable to equivalent 11/780 systems ($79K for a CI Package System and < $57K for an IDTC Package System as described on the next page vs. $50K for the VAX11/780 SV-AXCVA)

Maximize price/performance gain over 11/780 (at least 4 times 11/780 performance, warm floating point excepted)

IO architecture based on new Corporate interconnects (CI at FRS, NI on Unibus as soon as possible)

SBI capability for 11/780 compatibility

Design system for maximum dock mergeability

Maximize RAMP features

Minimize development cost

System Definition

Listed here are the basic elements of the two system kernel configurations upon which the Program is based. A CI Package System will be the principal system configuration and is expected to be the basis for all midrange and larger systems. The Integrated Disk-Tape Controller (IDTC) Package System, which will be available approximately three months after FRS, has a disk-tape controller within the CPU cabinet and is the basis for the smaller systems, although it too is expandable. Note that the integrated disk-tape controller is composed of current products - DW780 and UDA50 - just with new packaging and a special backplane; it involves no new hardware, and no new VMS software is needed. Note that the DMF32, the "Combo" board, has controllers for eight asynchronous lines, one synchronous line, and one line printer; which controllers are actually used depends on what other equipment is attached and what arrangements are made in terms of distribution panels for the various lines. Both system types contain a set of common elements that we shall first define as the "CPU kernel."

CPU Kernel

Processor and power system
1 LA120 console terminal
1 RL02 console load device
4 megabytes of MOS memory
1 SBI adapter (SBIA)
1 DW780 Unibus adapter
1 DMF32 Combo (8 asynchronous lines,
1 synchronous line, 1 line printer port)

CI Kernel

CPU kernel
1 CI780 CI adapter

IDTC (Integrated Disk-Tape Controller) Kernel

CPU kernel
1 IDTC DW780-UDA50
(4 disk ports)

From these basic configurations, the VENUS Business Plan defines a number of dock-mergeable packaged systems for handling the largest volume markets at the lowest cost. Unless otherwise specified, information in the present document pertains generally to the CI Kernel and systems containing it. The term "system base" refers to the base of any type of system.

The basic DMT system is the CI Kernel. The CPU Kernel (for DMT and similar purposes) is the processor plus 4 MB of memory.

Program Highlights

The System

High Availability

CPU Kernel - 99.5%

System base (including software) - 98.5%

No more than 1 software crash per month

MTBF (mean time between failures)

In each case the second number is the MTBF perceived by the customer, taking into consideration the fault tolerance of the CPU kernel and scheduling maintenance during off time. Figures include field performance data for the LA120 and RL02, but in VENUS these devices will have a lower duty cycle, which will somewhat increase the MTBF.

CPU kernel (DMT) - 1873/2058 hours
CPU cluster - 916/965 hours
CI Base - 415/427 hours
IDTC Base - 606/627 hours

VAX cluster system configuration possible

System MTTR - 3 hours; MDT - 5 hours

System installation and acceptance $\leq$ 48 hours

Warranty cost: CPU Kernel - $5823
CI Base - $14,399
IDTC Base - $9519

Maintenance cost (at 20th quarter of shipments)
CPU Kernel - $401 per month
CI Base - $1237 per month
IDTC Base - $689 per month

BMC (basic monthly charge) - TBD in Phase 2

Advanced RAMP features

Instruction retry

Multiplexers built into terminator chips for diagnostic inspection of all backplane signals

Diagnostic resolution to module in at least 95% of solid failures; resolution to chip level for RAM failures

All MCA chips and most RAMs mounted in sockets to allow field replacement

Integrated, intelligent maintenance/operator console (T-11 based)

Loopback diagnostics for IO controllers

User mode diagnostics

Etch backplanes (> 90%)

High reliability parts

Early warning on low voltage/high temperature

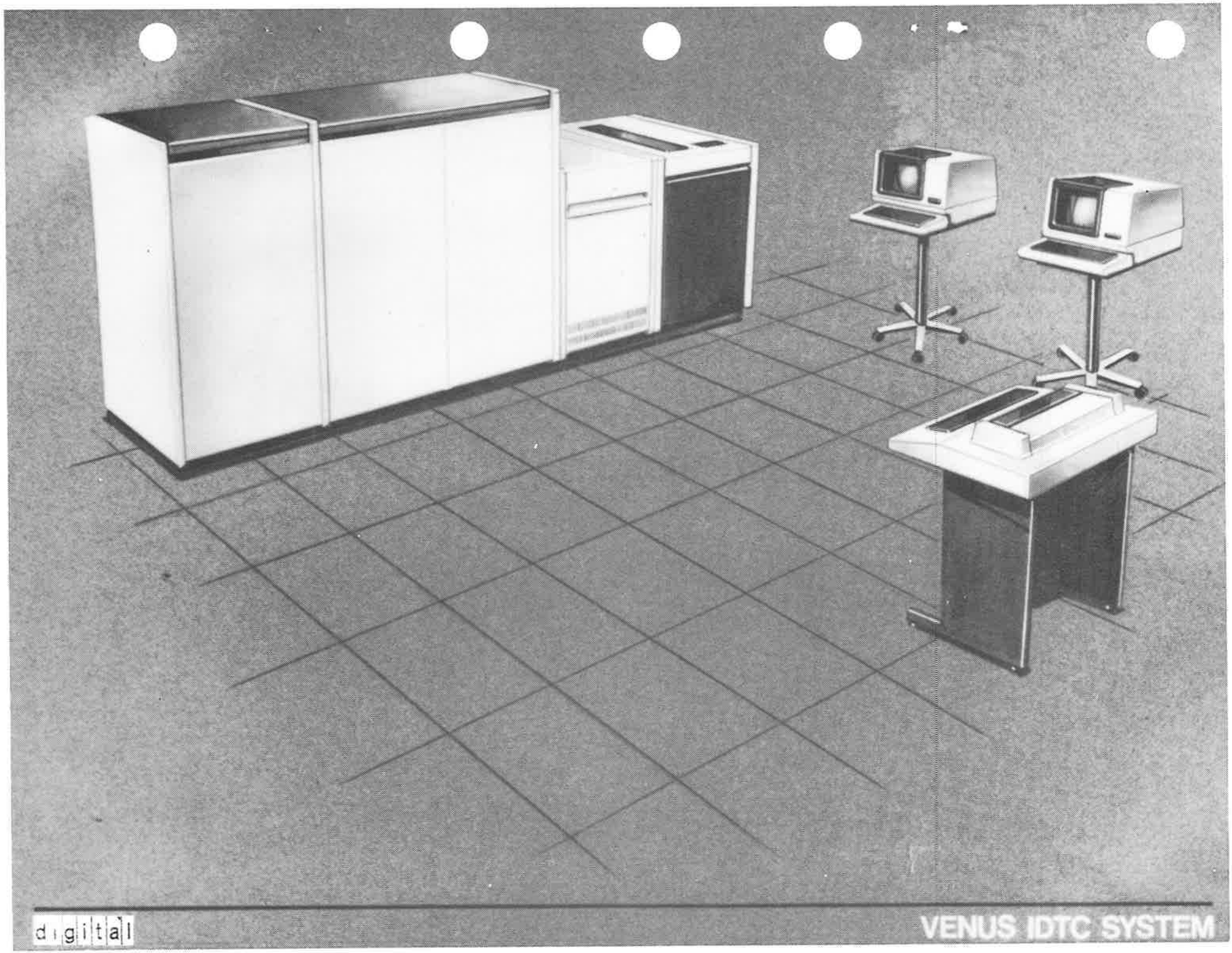
Power fail recovery

Remote diagnostic link

Battery backup on time-of-year meter (100 hours) and memory (10 minutes)

The Technology

Press pin, multilayer, controlled impedance backplanes (12 and 16 layers)


digital
VENUS IDTC SYSTEM

8-layer, controlled impedance L-type modules (4 signal layers)

Macrocell arrays (MCA) - Motorola Mosaic I ECL gate array LSI technology

Digital Hudson plant second source for MCAs

ECL 10K MSI/SSI and a few 10KH chips

Air cooled

Individual heat sinks mounted on each MCA

1K and 4K ECL RAMs

256K MOS RAM chips (64K MOS RAM chips to be used during initial prototype development only)

Corporate "switching regulator" modular power supplies

The Product

High end VAX system - corresponds exactly to the VAX architecture defined in the VAX System Reference Manual (DEC Standard 32); the AXE program, VMS and layered products will be used to verify the architecture

Many dock mergeable configurations

Absolute compatibility with VAX/VMS and layered software products for equivalent hardware (the medium for software distribution will be on 9-track 1600 BPI magnetic tape, and Product Management is pursuing the matter vis-a-vis the entire VAX family)

16K byte writeback cache with ECC

4 to 5 times VAX 11/780 performance

Instruction byte prefetch

Custom register file for A bus adapters

8K writable control store (there is no WCS option, but 1K is available to the user with limited support comparable to that on 11/780)

Optional floating point accelerator, 4 times 11/780 FPA performance

MOS memory in 4 MB increments to 32 MB

Supports new CI interconnect - in fact, the Program depends on the CI for HSC50 and VAX Cluster

2 taps on adapter bus for SBI adapters

VMS support for VENUS Processor initialization, error handling, IO adapters and console

PDP-11 compatibility mode (in software)

High volume fabrication, assembly and test

Cooling/packaging for class A environment (air conditioned, 15-32 degrees C, relative humidity 20-80%; raised floor preferred (for improved service profits) but not necessary

As defined in DEC Standards 60 and 62, the specific international regulatory needs for marketing the VENUS system in the data processing and telecomm line connect areas will be addressed. These needs include: RFI/EMI, Product Safety, Acoustics, and Telecomm, the last being primarily the responsibility of the applicable VAX development groups for the existing 11/780 comm options.

Power consumption

CPU cabinet: 5.6 kW, 19,125 Btu/hour, 8.62 kVa [CPU, FPA, 8 MB (64K chip) or 32MB (256K chip), console, 2 SBIA, 3 DW780s, 1 CI780]

Unibus-console cabinet: 1.1 kW, 3757 Btu/hour, 1.7 kVa (RL02, BA11, 1 DMF32, etc.)

System fully DMTed and PMTed

Meets or betters European noise standard (60 dbA), and we will deal aggressively with vendors concerning noise requirements for peripherals

Will provide a strong functional base for:

High end real time
Foreign device connect
Transaction processing
Timesharing
Batch
Distributed processing
Distributed data base management

When and How Much?

The individual VENUS managers and supervisors have identified the various tasks and events that make up the overall Program and have determined reasonable schedules for implementing them. Combining these schedules and taking into account their interdependencies results in the following dates:

CI Packaged System FRS June 1984
Transfer cost: $79K

Floating Point Accelerator FRS June 1984
Transfer cost: $ 4K

Dual SBI System FRS Oct 1984
Transfer cost: configuration dependent

IDTC Packaged System FRS Oct 1984
Transfer cost: < $57K

It should be noted that the above are the times at which the Program will have the various products ready for FRS. Because of Marketing considerations however, Product Management may in some cases prefer actually to make them available at a later time.

1.2 WHY VENUS?

In every category - from market suitability to customer satisfaction, from cost/performance to expansion capability - VENUS is the computer for the high end of the VAX line in the mid-eighties. It is also consistent with the Corporate strategy of settling principally on a 32-bit architecture by 1985.

Leadership

In terms of performance, availability, cost of ownership, and range of applicability, VENUS is a major stride both within Digital and in the industry as a whole. These exceptional improvements are due in part to use of state-of-the-art Mosaic I ECL array technology.

VENUS will be the most powerful system in Digital's VAX product offering, with higher availability and lower cost of ownership than any comparable Digital system. With the layered software products planned for delivery in the early eighties, VENUS will meet the needs of a broad range of technical, commercial, and

special-application customers. By incorporating the latest technology in hardware and software, VENUS will bring "people oriented" computing to performance levels never attained before.

Cost/Performance

VENUS-based systems will track the cost/performance improvement shown by the computer industry as a whole. Thus in raw cost/performance terms, VENUS can be expected to be as competitive in the mid-eighties as the 11/780 is today; furthermore, in functionality terms, our large software development for VAX systems will make VENUS systems even more attractive.

Performance

On computation-limited workloads, VENUS will have 4 times the throughput of a comparable 11/780. On disk IO-limited workloads, the improvement will depend principally on the capability of the HSC50. Within the mechanical constraints (and most IO limits are mechanical), the SBI-CI-HSC50 subsystem is capable of considerable data-transfer optimization; but beyond this, the HSC50 also has features for optimizing the mechanical operations of the disk itself. On terminal communications limited workloads, VENUS with DMF32's will support character throughput rates in excess of 100,000 characters per second.

Cost

The cost of ownership of VENUS systems will be equal to or better than comparably configured 11/780 systems.. "Comparably configured" means that VENUS main memory and disk capacity are four times those of "comparable" 11/780s. We expect to reduce FA&T costs by dock merge of many systems and offering packaged systems, and to minimize life cycle cost by careful design of the system, its RAMP features, and our service and manufacturing strategies.

Market Suitability

VENUS will span two very different market places: as a small mainframe, it will be comparable in performance to a 370/168; as a high end minicomputer, it will pick up the real time, interactive,

and distributed processing applications as they grow to higher throughput requirements. Although initially most appropriate to midrange scientific computation markets, VENUS will be able to take full advantage of VAX/VMS software efforts to penetrate commercial ADP applications. Over its life, VENUS is expected to be installed in roughly as many commercial as scientific applications.

Timeliness

The 11/780 is presently under fire from many directions - the IBM 4331 and 4341 (and recently announced 3083E), the SEL 32/87xx series, the Interdata 3240, and expected offerings from DG and HP are all aggressive products in the 11/780 market space. VENUS's market introduction in 1984 will provide Digital with a resource to meet these challenges.

Flexibility

While VENUS's high marks in performance, cost and other characteristics make it an excellent instrument for attacking new markets and attracting new customers, its compatibility not only with VAX/VMS and all VAX layered software products, but also with the PDP-11 will make it exceptionally attractive to present customers for upgrading and networking.

Customer Satisfaction

Low component count, design that anticipates exceptional conditions, and extensive checking circuitry give VENUS high inherent reliability. Ride-through strategies to survive transient errors help minimize vulnerability to intermittent failures, and error logging gives Customer Service the information to locate and repair such faults. The diagnostic logic supports module-level fault isolation, and in many cases isolation to chip level. These and other RAMP features contribute directly to customer satisfaction, as does the resulting lower life cycle cost.

Interconnectability

VENUS will interface to existing and anticipated applicable Corporate interconnect mechanisms. Easy access to traditional Unibus and Massbus devices will be available.

Multicomputing

VENUS processors can be loosely coupled via the CI, e.g. the VAX Cluster configuration. With full exploitation of the Corporate interconnect strategies, VENUS can lead the real computer revolution of the eighties - using arrays of $350K machines to solve multimillion dollar problems.

2 THE SYSTEM

A VENUS System is more than just hardware - it is also the software that makes the system go, and its performance characteristics and RAMP features, all of which we consider here.

2.1 LOGICAL ORGANIZATION

In the block diagram of the central part of the system, Figure 2.1, the processor contains the five blocks interconnected by the diagnostic bus: the single block in the upper left and the upper four blocks in the center column. These four blocks represent the instruction or I box, the execution or E box, the floating point accelerator FPA (also called the F box), and the memory control or M box. The last of these provides the connecting link to both memory and the IO subsystem, whereas the upper three blocks comprise the "processing" part of the processor.

The heart of the entire system is the instruction box, which receives the instruction stream of bytes from memory, and from it determines what other information to retrieve and what activity to initiate in the E box. The execution of each instruction is done in four stages, with the I box handling the first three: fetching the instruction, calculating the required addresses, and fetching the operands. It then turns the execution of the instruction over to the E box, but at the same time it helps to speed up overall operation by starting to work on the next instruction. The E box, based on a binary/BCD ALU, carries out whatever logical, arithmetic and other operations are required to execute the instruction, after which it sends to the I box any results that are to be written in memory. If the optional FPA is included, the E box uses it to speed up the execution of floating point instructions, but from the point of view of the I box, the FPA is simply an extension of the E box. Basic to

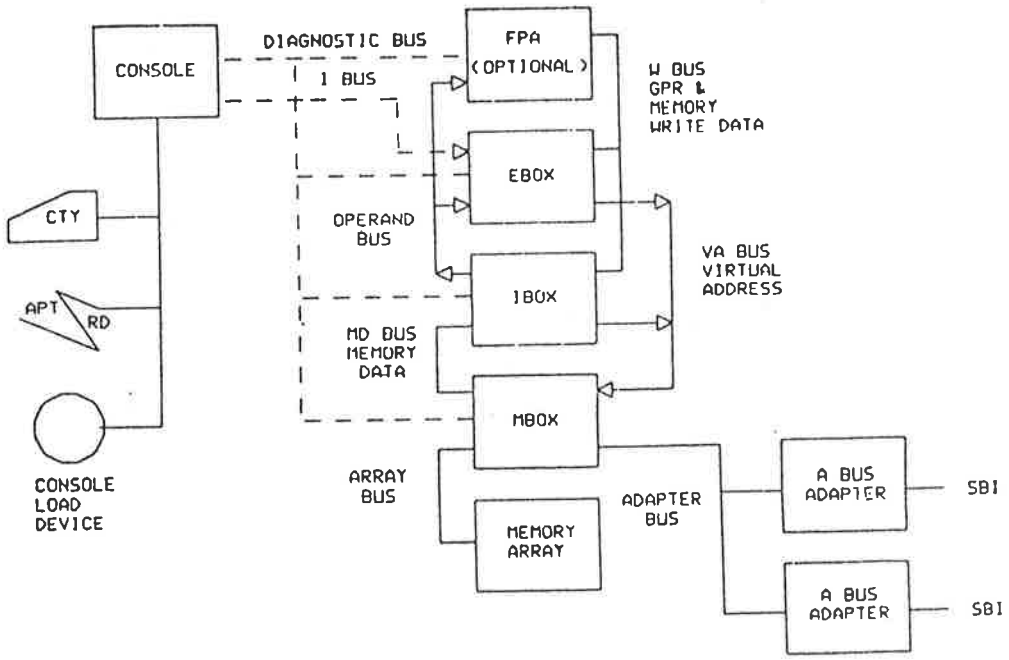


FIGURE 2.1 VENUS PROCESSOR LOGICAL ORGANIZATION

the accurate and fast manipulation of data are the general purpose registers (GPR), of which each of the three boxes has one or two sets of sixteen. Altogether five copies of the GPRs are kept to guarantee very fast and flexible access and instruction retry.

Interconnecting the various boxes are a number of buses. All movement of data between the processor and both the memory array and the IO subsystem occurs via the MD bus that connects the M and I boxes. Over this bus the I box receives the I stream and the memory operands. It passes the latter on to the E and F boxes over the operand bus. Results from either of these boxes are sent via the W bus to the I box, which in turn passes them on to the M box over the MD bus. The W bus is also used for keeping the five sets of GPRs identical to one another. Both I box and E box can supply addresses (almost always virtual) over the VA bus to the M box. All buses and registers handle 32-bit longwords.

Also contained in the processor is a micro-processor-based console, which is connected to all four of the boxes by a serial diagnostic bus. The console provides the system clock, a time-of-year clock, and environmental monitoring. Associated with the console are a local LA120 terminal for use by the operator, an RL02 removable disk (mounted in the Unibus cabinet) for bootstrapping and diagnostic activities, and a remote diagnostic link which can be utilized by an APT window. Bootstrapping is done by the console passing initializing and setup information in bytes to the various boxes over the diagnostic bus. The 8K x 84 bit control store for the microcode is in the E box, but each of the other boxes has a small control store to hold special microcode for its own operations. Also connecting the console to the E box is the C bus for communicating with the software and performing console functions.

The M box includes a 16K-byte data cache, error detection and correction circuits for the cache and memory array, and microcode-driven control logic for governing communication with the IO subsystem as well as handling memory. The control part includes special byte write logic to speed up the insertion of bytes in longwords, and refresh logic for the MOS RAMs in the array. Connection to memory is via the array bus, and to the IO subsystem via the adapter or A bus. Each array board contains four MB of MOS storage; a typical memory is four to eight MB, with expansion to 32 MB possible. It is possible that within two years after FRS, memory density will improve by a factor of four (the addressing capability of the processor hardware is 512 MB). IO bandwidth is significantly increased

over 11/780 by removing all CPU-memory traffic from the SBI. There can be no SBI memory, and there is no support for a device like the MA780.

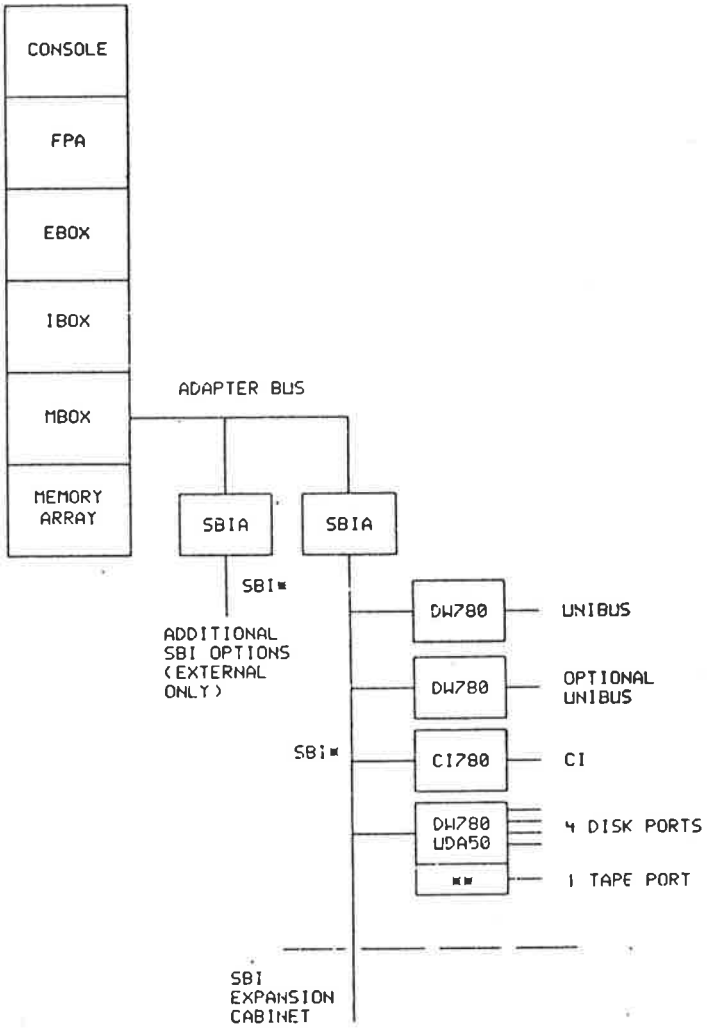
Although the FPA is optional and memory size is variable, most variation from one system to another occurs in the IO subsystem. Such variation is considerable, including both the interconnects and a large variety of peripheral equipment, but in general system configurations are of two fundamental types, based either on the CI Base or the IDTC Base. The basic constituents of these systems are shown in Figure 2.2. Available initially will be systems built on the CI Base, where the IO subsystem has an SBI with units that interface to a Unibus and a CI. The latter has fifteen nodes that allow connection to HSC50 disk or tape systems, and to other computers in a multicomputer system. For a smaller scale system, the IDTC Base has an integrated DW780-UDA50 disk-tape controller instead of the CI780. Either system can have a second Unibus adapter in the CPU cabinet; more adapters, including the RH780 and DR780, can be added outside the cabinet; and a second SBI can be installed to handle the external adapters and thus share the load.

2.2 PHYSICAL ORGANIZATION

Figure 2.3 shows the physical layout of the CPU cabinet. In terms of general organization - position of backplanes, power supplies, cables, blowers, etc. - the layout is the same for all systems. Viewed from the front, the left half of the module area is a single CPU card cage containing two backplanes for memory and processor, both implemented in L-type modules. The left backplane accomodates eight memory array boards of four MB each. Beside the memory is the processor, which if the optional floating point accelerator is included, requires seventeen modules.

CPU Box	Number of Modules
I box	4
E box	4
System clock	1
Control store	2
M box	3
FPA	2
Console	1
Spare	1

Modules with MCAs are one inch apart; other CPU modules use 0.6 inch spacing. Memory array modules use 0.5 inch spacing.



* ONLY ONE SBI CAN LEAVE THE CPU CABINET

**TU81 TAPE DRIVE AND CONTROLLER ARE REQUIRED TO CONFIGURE IDTC SYSTEM

FIGURE 2.2 BASIC SYSTEM CONFIGURATION

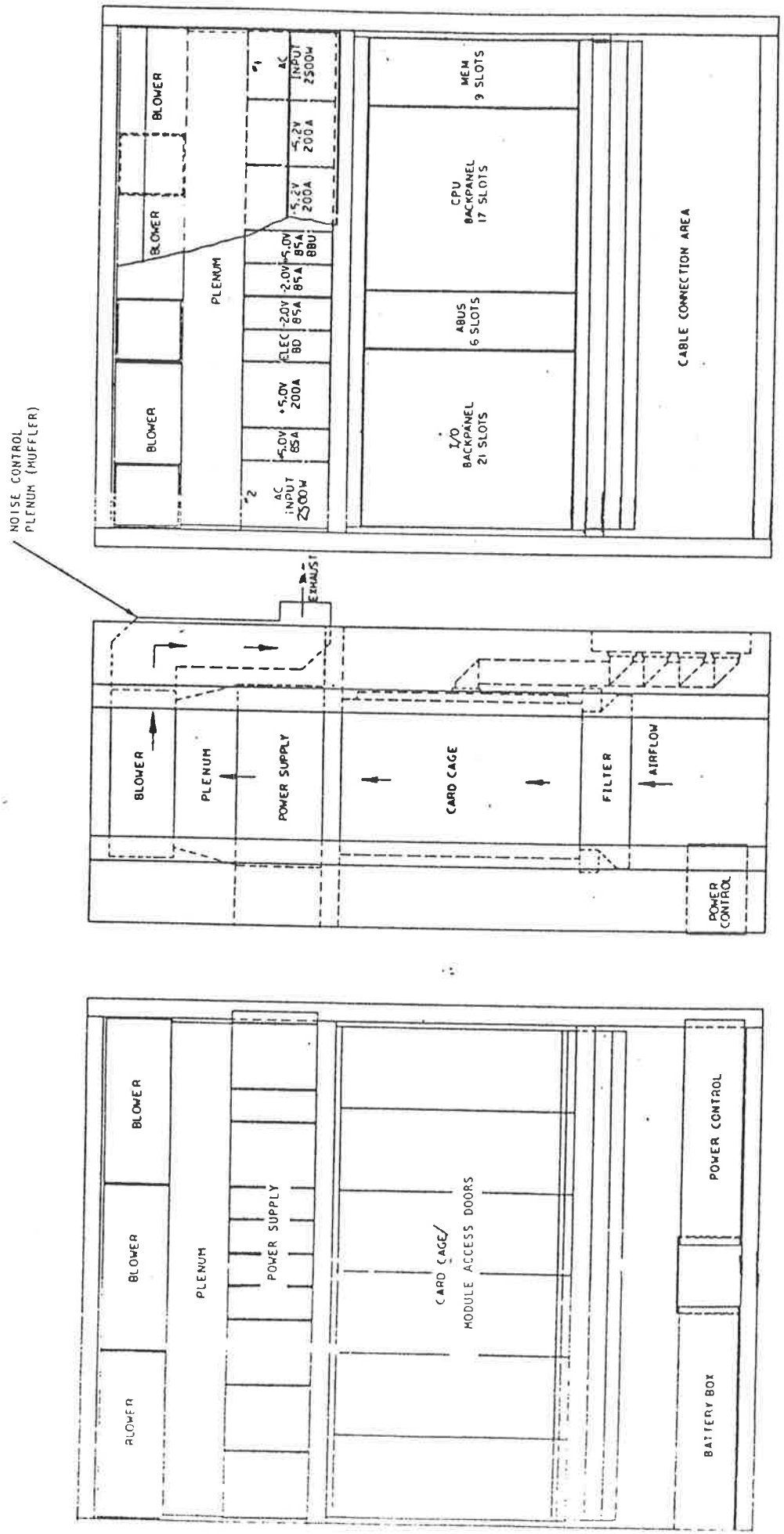


FIGURE 2.3 CPU CABINET CONFIGURATION

The right half is also a single card cage containing the small A bus backplane and the larger IO backplane; this entire cage could be replaced for special applications or to implement an IO oriented mid-life kicker. The A bus backplane (on the left) has space for two SBI adapters of two L modules each (the first SBIA is plugged in at the farther end from the processor) The IO backplane accomodates a mixture of hex, extended hex and L modules for the adapters on the internal SBI. This backplane contains one DW780, space for a second, optional DW780, and either a CI780 CI adapter or a DW780-UDA50 Integrated Disk-Tape Controller (The system is designed to allow a single system to have both when desired). Any adapters beyond these must be mounted outside the CPU cabinet; such adapters can include the DR780 and RH780 as well as those available in the CPU cabinet. In any system a single SBI can handle all adapters, or a second SBI can be added to handle the external ones (i.e. only one SBI can leave the CPU cabinet).

In systems built for shipment outside the United States and Canada, there will be a 18 kVa transformer to interface with the numerous variations in available utility voltages. This transformer is mounted at the bottom of the front-end cabinet at the left of the CPU cabinet. Voltage conversion requirements for Unibus expansion cabinets, SBI expansion cabinets and the like will be handled in the fashion determined by the groups responsible for their design.

Cabinet Arrangements

Every system has a front-end cabinet attached to the left side of the CPU cabinet viewed from the front. Besides typical Unibus communication and unit record controllers, this cabinet (Figure 2.4) contains the console load device and the stepdown transformer wherever that is necessary. If additional Unibus cabinets are required, they are bolted on at the right. If external adapters are needed, they are installed in one or two SBI expansion cabinets (four per cabinet) attached at the right of the CPU cabinet, between it and any additional Unibus cabinets. Cabinets for Unibus disks and tapes are attached at the far right. CI and Massbus devices can be attached at the right or placed separately elsewhere in the computer room.

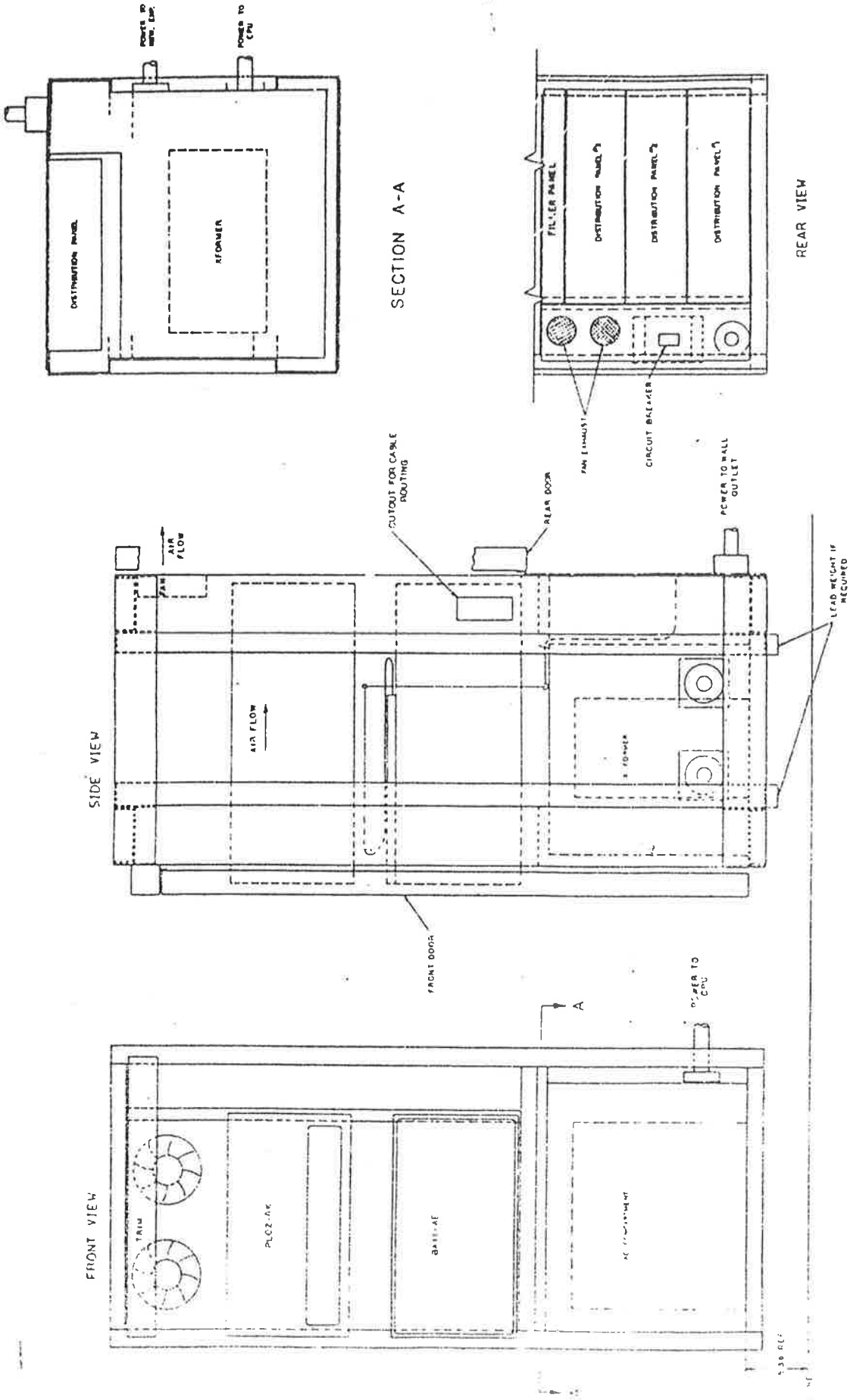


FIGURE 2.4 UNIBUS-CONSOLE CABINET CONFIGURATION

2.3 PERIPHERAL EQUIPMENT

The peripheral equipment includes both new and current products in all categories: interconnects, adapters, controllers, and individual IO devices.

Interconnects

VENUS configurations are based on system interconnects reflecting Corporate strategies. The characteristics and status of these interconnects are given below; all have high data integrity and provide appropriate electrical isolation.

SBI Synchronous Backplane Interconnect - present VAX-11/780 interconnect to Unibus, Massbus and other adapters; high bandwidth, medium cost.

CI Computer Interconnect - joins loosely coupled computers, and mass storage; high bandwidth, 16 nodes; under development

SI Storage Interconnect - joins disk and tape drives to controller; high bandwidth; being tested (the interface to the SI is the standard disk interface, SDI, and several disk projects are being based on it).

NI Network Interconnect - joins computers, work stations, intelligent terminals, etc., in local network; moderate bandwidth, 100 drops per segment.

Adapters

These interface the A Bus to the SBI or the SBI to subsidiary interconnects such as the CI and Unibus.

SBIA SBI adapter on A bus, scheduled and funded.

DW780 Unibus Adapter - current product.

CI780 CI adapter, scheduled and funded.

DR780 High Speed Block Transfer Port for customer equipment or CPU-CPU communication; current product.

RH780 Massbus Adapter - current product.

Controllers

Two major controllers are expected to be utilized in the VENUS system. Minor controllers, such as for unit record equipment, are included with the devices themselves.

HSC50 Hierarchical Storage Controller - intelligent mass storage controller on the CI; contains six subcontrollers for SDI disks and tapes; unit has many RAMP and high-performance features; project funded with FRS scheduled for Q4/FY83.

UDA50 Intelligent mass storage controller on the Unibus; contains four subcontrollers for SDI disks; some RAMP and high-performance features; current product.

Recommended IO Devices

Following are those products currently in development that we believe are critical to the success of VENUS. Current products we intend to support are listed at the end of Section 3.6.

RA60 removable disk on SDI, 200 MB capacity.

RA81 fixed disk on SDI, 456 MB capacity, 3 MB per second maximum transfer rate.

TA78 tape, 1600/6250 bpi, 125 ips, HSC50 controller.

TU81 tape on Unibus, 1600/6250 bpi, 75 ips.

2.4 SOFTWARE

As far as the software is concerned, the most important thing to keep in mind is that VENUS is a VAX processor, that its operating system is VMS, and that there is only one version of VMS for all VAX processors. VMS development operates under two fundamental requirements: that no matter what processor the single version of VMS is booted on, it shall be capable of configuring the support for that processor automatically and transparently; and that a user program or higher level system program that runs on any VAX processor shall run on all. As shown by the examples in the chart below, the many elements that constitute the complete VAX software package are organized into three layers that are superimposed or built upon the VAX hardware.

Unbundled (Layered) Products

Fortran	Basic
Cobol	Pascal
PL/1	Coral-66
RPG	APL
DIBOL	C
ADA	Pearl
DSM	DBMS
Datatrieve	Data Dictionary
Enhanced Terminal Handling	Forms Management
	Office Automation
Transaction Processing	Software Development Tools
Internet Communications	

Bundled Products

Text Editors	Macro Assembler
Linker	Debugger
Command Languages	Batch Processor
Spoolers	Sort/Merge
Run Time Library	SYSGEN
Error Log Analysis	RMS
Backup	DECnet

Executive

Scheduler	Device Drivers
System Services	IO Adapter Support
Memory Management	Error Handling
CPU Initialization	RSX Compatibility

In this structure, the bundled products are those programs that are intimately associated with the executive and that together with the executive constitute the basic software necessary for effective operation of the system. The higher level products in the unbundled layer (usually themselves referred to as the "layered" products) maintain a certain independence of the operating system, in that they are developed, released and sold separately. Such organization naturally requires that any changes in the lower layers be made in an upward compatible way. Unbundled products are not done directly by the VMS Group.

In terms of VENUS software, it should be noted that processor dependencies are visible almost exclusively to the programs in the executive layer. Moreover any features or enhancements added to the layered products for VENUS automatically become available to all VAX systems.

2.5 PERFORMANCE

The overall CPU performance goal of VENUS is between four and five times that of the VAX-11/780. This will be achieved by performance oriented features in the Processor itself, in the Floating Point Accelerator, in Memory, in the Peripheral Subsystem, and in Software.

Processor

In comparison with the 11/780, the processor speed is improved by:

1. A reduction in the cycle time from 200ns to 73ns. Even if the structures were identical, this would provide an improvement factor of 2.7 over the 11/780.

2. The pipelining provided by the parallel operation of the IBox and EBox. The improvement factor is dependent upon the instruction mix and is greatest when the branch and character string instruction frequencies are low.

Floating Point Accelerator

The EBox normally executes the floating point instruction set with microcode (warm floating point) and this exhibits performance in the same order of magnitude as a VAX-11/780 equipped with an FPA. The VENUS FPA provides hardware enhancement to the EBox with the result that floating point instructions are executed between 8.5 and 1.6 times faster than the "warm floating point" versions (depending on instruction). The unweighted average is an improvement of 4.3. The improvement in performance seen by the user is therefore dependent upon the mix of floating point instructions used.

Memory

1. The memory interface to the CPU and I/O is through the 16KB cache and is controlled by the MBox. Hit-ratio improvements over the 11/780 are not only attributable to the doubling of the cache size, but also to the cache's being structured as two-way associative with flushing done on a least recently used basis.

   Cache-to-memory write activity has also been reduced significantly by using the write-back

instead of the write-through technique. In this case, memory writes are performed only when the data is modified and the cache location is needed by a current operation.

The cache and memory times are as follows:

	VENUS	11/780
Main memory read access	533 ns	1400 ns
Write cycle time	73 ns	200 ns
Cache cycle time	73 ns	200 ns

The aggregate effect of these cache improvements is again dependent upon the instruction mix and memory usage.

2. Not only has the memory cycle time been reduced considerably, but once a write cycle has been started in one array board, the MBox can initiate a second write in another. Timing is such that different array boards can absorb writes as fast as the MBox can request them.

Performance Modeling Results

The VENUS CPU model measures the number of cycles any benchmark takes to run while executing in USER MODE. It accurately models cache activity and fully measures the effect of varied instruction streams encountered in the different benchmarks. It does not measure the translation buffer activity nor effects due to interrupts. Equivalent performance measurements of an 11/780 system were made by averaging execution times on a lightly loaded 11/780 system.

The following comparisons of improvements in execution times have been measured:

Benchmark	Improvement over 11/780	Benchmark Characteristic
Whetstones	5.1	Single Precision Floating Point
Prime	5.4	Integer Calculations
Hanoi	4.26	Conditional Branches

NOTE: If design problems are encountered, schedule will be treated with a higher priority than system performance.

Peripheral Subsystem

The overall performance of the IO subsystem depends both on the performance of its individual parts, and also on the characteristics of processor and memory, as the peripheral adapters and controllers interact so much with them. For a typical mix of traffic, the memory burst bandwidth on the A bus is 13.1 MB per second with one SBIA, 17.1 with two (for details refer to the IO Plan). The frequency of interrupt checking will be greater than in the 11/780, reducing both the latency and the worst-case wait. The following table gives the peak transfer rates in megabytes per second for the various units in the IO subsystem.

SBIA		13.1
DW780	1.5	
CI780	3.5	
DR780	6.67	
RH780	2.2	
SI		3.125
HSC50		6.25
		(3.4 MB sustained)
Disk	3.125	
Tape	2	
UDA50		1.77

Maximum A bus bandwidth with two or more ultra high speed adapters using octaword transfers would be 33.3 MB per second.

Software

Software performance depends not only on the activities of those who create the software, but also on the performance of the hardware on which it runs. Hence the most direct improvement of VMS as an operating system for VENUS will be the improvements in processor speed, memory size and speed, and IO capabilities of VENUS as against the 11/780. On the other hand, each release of VMS has goals for quality, functionality and performance, among others, to varying degrees. VENUS will usually benefit from performance enhancements engineered for the whole VAX family.

2.6 RAMP AND DATA INTEGRITY FEATURES

Features to guarantee the integrity of the data in the system and to promote its reliability, availability and maintainability are built into VENUS at every level: they range from minor characteristics of

individual circuits to major provisions embracing the entire system. Some of the more significant features are these:

Inherent reliability achieved through low component count, worst-case logic design, and high reliability parts.

Dynamic monitor error reporting, by means of an error logger, to aid in identifying the source of an intermittent failure. This logger will be used for both hardware and software malfunctions. The log is kept in a disk file.

Instruction retry whenever it is appropriate to the error type. For example five copies are kept of the general purpose registers. Hence on a GPR parity error, the instruction can be repeated using a different copy.

Additional software features in this area include automated patching and updating procedures, powerfail-restart support, user mode diagnostics, extensive protection facilities, and dynamic memory configuration to exclude bad pages.

Parity checking at all RAMs and buses, and parity continuity carried through all major data paths. Parity is kept not only for data, but also for physical addresses and the microcode.

Separate selects to each memory array board, so the control logic for storage selection is all in one place, and faults can be isolated to an individual board.

Single bit error correction and double bit error detection for the cache and memory array, with automatic rewriting of the corrected word.

Memory battery backup for ten minutes. Backup can be set shorter to save on battery recharge time, thus allowing user to choose riding out several short power failures at the cost of going down during a long one.

The FPA does continuous self-testing when not being used by the application.

The ability to reconfigure the system without the FPA when experiencing floating point failures.

Fast, accurate diagnostics, with first-failure fault isolation to field replaceable unit in CPU cluster and to module in peripherals.

Error logic for monitoring all backplane signals from the console via the diagnostic bus.

A "keep alive" count kept by the console to determine if the system is hung. Should the hung condition be detected, the console saves the state of the machine.

Other console diagnostic features, including remote capability, flexible clock control, and some visual indicators should the console be unable to report its own failures.

Extensive console and EMM monitoring of the environment and the power system.

VENUS will be configurable in clusters using all high availability features being developed for VMS V3B.

3 DEVELOPING THE SYSTEM

The VENUS Program is organized around a strategy for developing a complete computer system. This strategy has a number of stages, and it is accompanied by phase reviews and thorough program tracking, with major milestones pinpointed. The process culminates in the marketing of two classes of systems at specific times. There are of course risks attendant on the development process, and these are duly noted.

Almost all of the staff and all key personnel are already in place. Figure 3.1 illustrates the Program organization.

3.1 DEVELOPMENT STRATEGY

The overall strategy is to develop a system whose IO subsystem is based on the SBI, using the CI for mass storage and the Unibus for communications and unit record. However, employment of a Unibus-UDA50 integrated disk-tape controller in place of the CI will allow systems at lower cost with moderate IO performance. The reasons for taking this approach are several:

SBI and the Unibus form a known, well-defined bus structure with mature software, and the CI with its mass storage peripherals is well enough along so we can depend on it with confidence.

Improved cost/performance ratio of CI-HSC over Massbus in medium-to-large system configurations.

Better chance of meeting FCC and acoustic goals with CI peripherals.

Satisfy current 11/780 customers via upgrading.

Offer Unibus and Massbus upgrades.

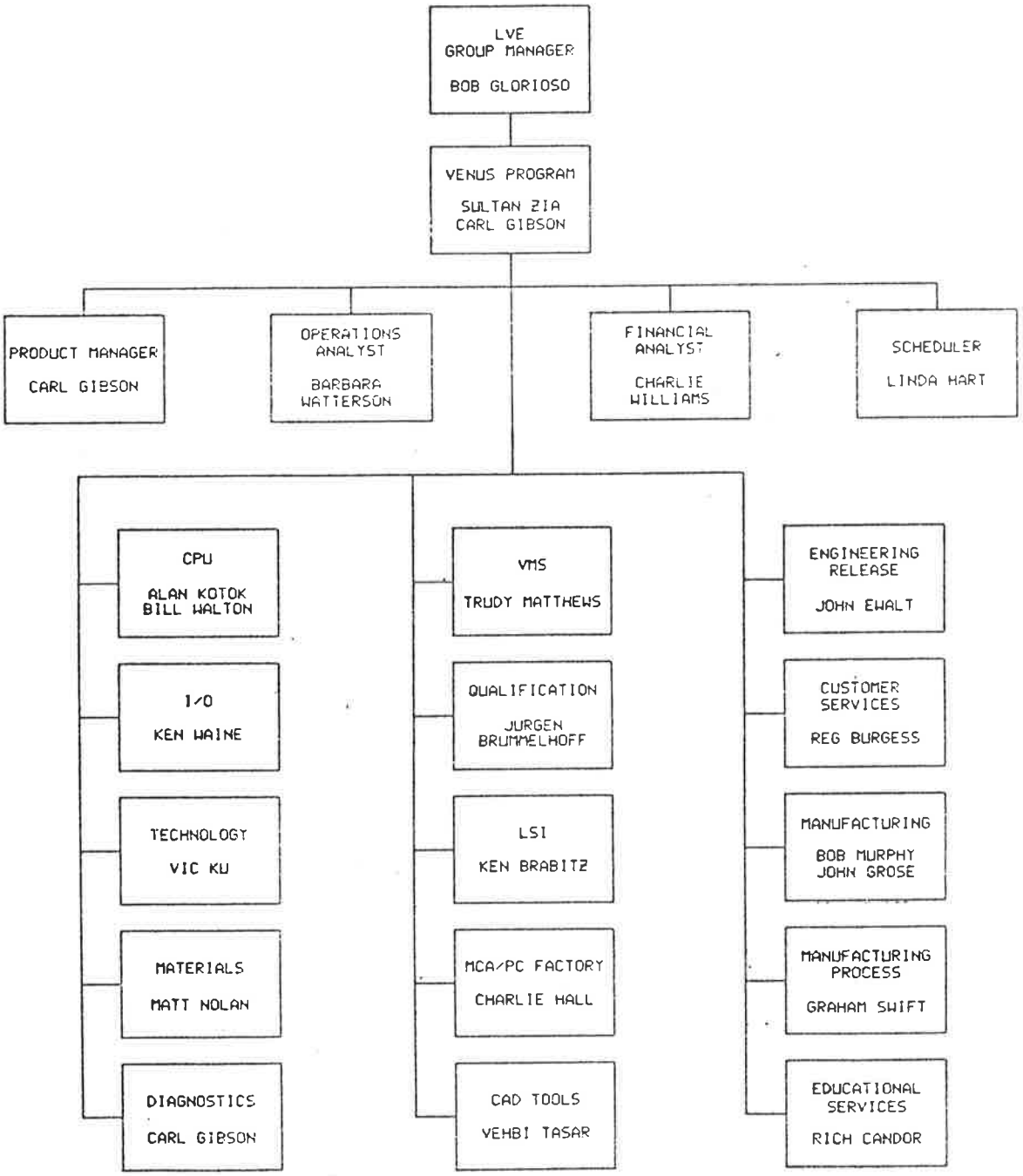


FIGURE 3.1
VENUS PROGRAM ORGANIZATION

The VENUS development strategy is organized in the following seven stages:

1. System Performance Analysis

   The VENUS Program is funding a two-person effort in the SPA Group in Hudson to do system and IO performance analysis and system modelling of VENUS. This work use benchmarks and workloads to determine whether functionalities of the different parts of the system are consistent with one another, e.g. are there any bottlenecks? is there enough IO bandwidth? Results to date indicate that VENUS CI systems configured with adequate memory and disk can support up to 320 users, and IDTC systems up to 96 users, running the ECS heavy workload.

2. Design Verification/Validation

   VENUS Design Validation has as its goal the validation of the VENUS design before hardware prototype power-on (February 1, 1983). This design validation involves the verification that the VENUS design "performs correctly" from an architectural and organizational perspective (behavioral verification) and that all timing constraints are met (i.e., that no path has either too long or too short a delay associated with it and that no timing errors are present). In our current strategy these two efforts, behavioral verification and timing analysis, have been de-coupled and are proceeding independently. However, the hardware build and prototype power-on phases of the VENUS project are contingent upon the successful completion of both tasks.

   In this section we shall give a brief overview of the problem of design validation, describe the tools being used in this process, and present some models that will help the reader to understand the complexity of the problem. For further and more detailed information on anything discussed here, the reader is referred to: Colon Osorio et al, "VENUS Design Validation Plan," Internal Memorandum, Master Revision 0, June 14, 1982.

Problem Definition

o Custom LSI design provides the designer with:

1. Higher densities
2. Improved performance over MSI/SSI designs
3. Lower power dissipation

at the cost of:

Design Turnaround Times

o This is due to:

1. A rigid design medium (the custom LSI part)
2. The lack of an interactive debug mechanism
3. The high cost of error correction (4-8 weeks for Motorola MCAs)

o As a consequence, design verification/validation of the VENUS processor via a hardware vehicle (prototype) would render the design obsolete by the time it was ready for shipment, and hence:

o This new Design Verification/Validation Plan, utilizing a hierarchical model and software simulation tools, was put into place. The hierarchy has three levels, as shown in Figure 3.2. The tools and their functions are described below:

1. TUMS Functional Simulator - to be used primarily as a microcode debug tool at the box level, and as both a microcode debug and functional (architectural) debug tool at the CPU level.

2. SAGE Logic Simulator - to be used as a logic validation tool at all levels in the hierarchy. The VENUS SAGE model is the closest approximation to an actual breadboard.

3. Timing Verifier (AUTODLY) - to be used separately as an analytical tool for validation of critical timing paths.

Functional Validation

Validation is an analytical process used to compare two models. In previous design efforts (see Figure 3.3), validation was considered to be the process of testing both the user apparent architecture of a processor (e.g., VAX-11)

and its organization (e.g., VAX-11/780 print set) by running tests on the prototype. In this context, functional validation corresponds to the validation of relationships (a) and (c) of Figure 3.3. In this model, the set of tests (e.g., AXE) running in a hardware implementation assumed correct (VAX-11/780) was used as the reference model to which the new hardware was compared.

Note that the purpose of the validation process is simply to find the differences between the two models being compared. Furthermore, the fundamental assumption of the validation process is that one of the models being compared is correct, and that therefore any differences between the two models represent design errors.

However, current design technology makes it prohibitively expensive to use a hardware model in the VENUS validation process. Instead, Figure 3.4 illustrates how the hardware model is replaced by a gate level simulator model (SAGE model) and a behavioral model (TUMS model). In addition, due to the English nature of the VAX-11 SRM, AXE running on the VAX-11/780 is used as the reference "correct" model. In Figure 3.4, the classical validation process of Figure 3.3 is replaced by TUMS and SAGE models of the hardware. These are used to validate the hardware's "VAXness" (relationships (g) and (j)) and its "VENUSness" (relationships (d) and (e)).

Timing Verification

In order for a digital system to perform correctly, a designer must take into account the possible propagation delays associated with each of the elements of the system, from MCAs to individual boxes, to the entire CPU. If a path through the system has either too long or too short a delay associated with it, then the value of the circuit may be wrong at a critical point, causing it to calculate an incorrect result, in other words causing a timing error. AUTODLY is an analytical tool, not a simulator, designed to uncover all such timing problems in the VENUS design. Hence, as design is completed, AUTODLY will be used to verify all timing paths on the VENUS CPU and to validate all timing constraints.

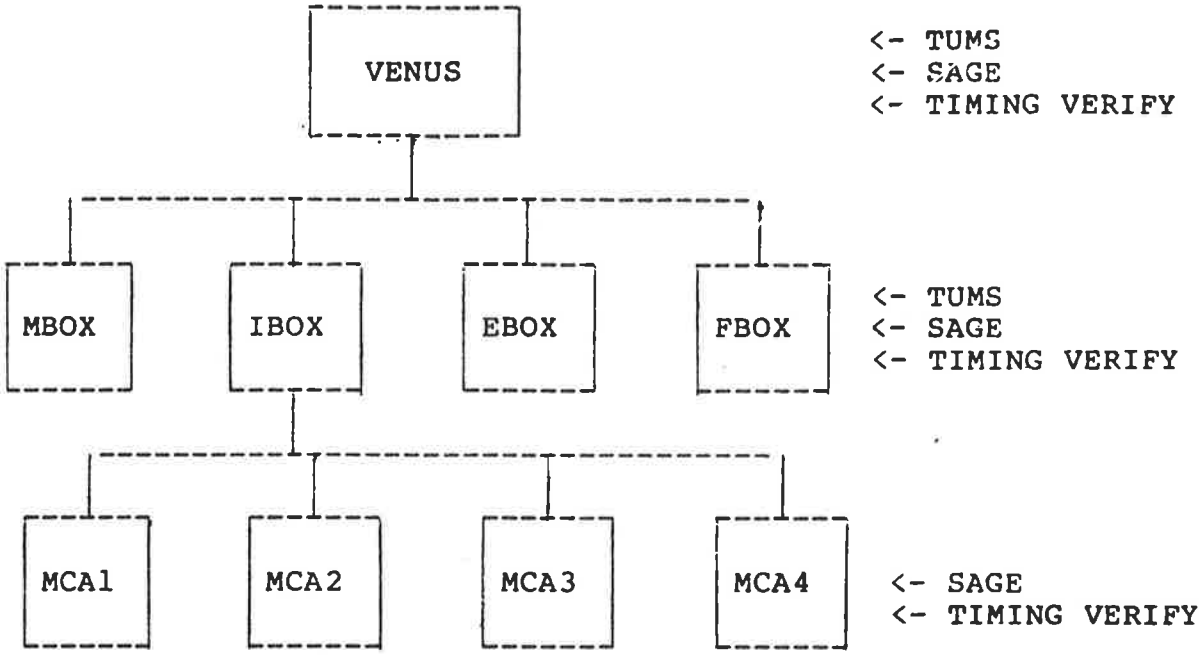


Figure 3.2 Design Verification Strategy for Venus Processor

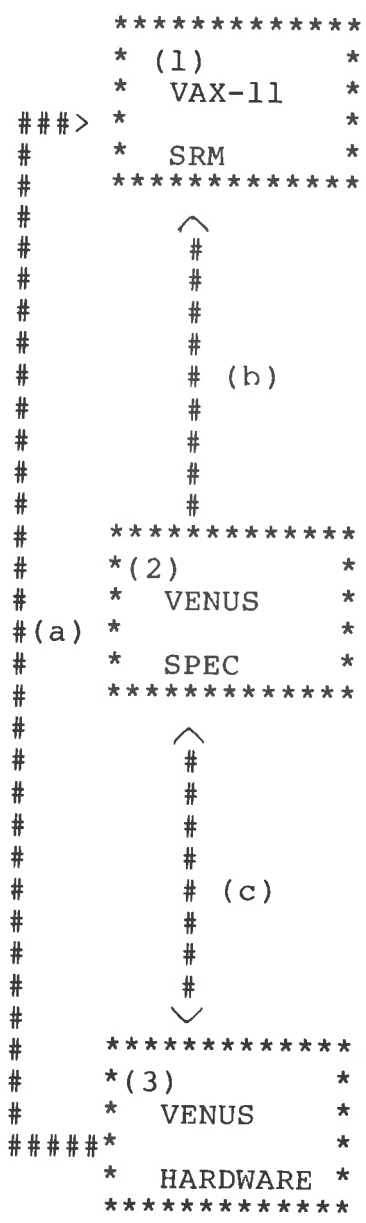


Figure 3.3 VENUS Hierarchical Model for Design Validation

(a) VENUS HARDWARE is a superset of the VAX-11 SRM (i.e., 3 ==> 1)
(b) VENUS SPEC is a superset of the VAX-11 SRM (i.e., 2 ==> 1)
(c) 1:1 correspondence between VENUS SPEC and VENUS HARDWARE (i.e., 2 <==> 3)

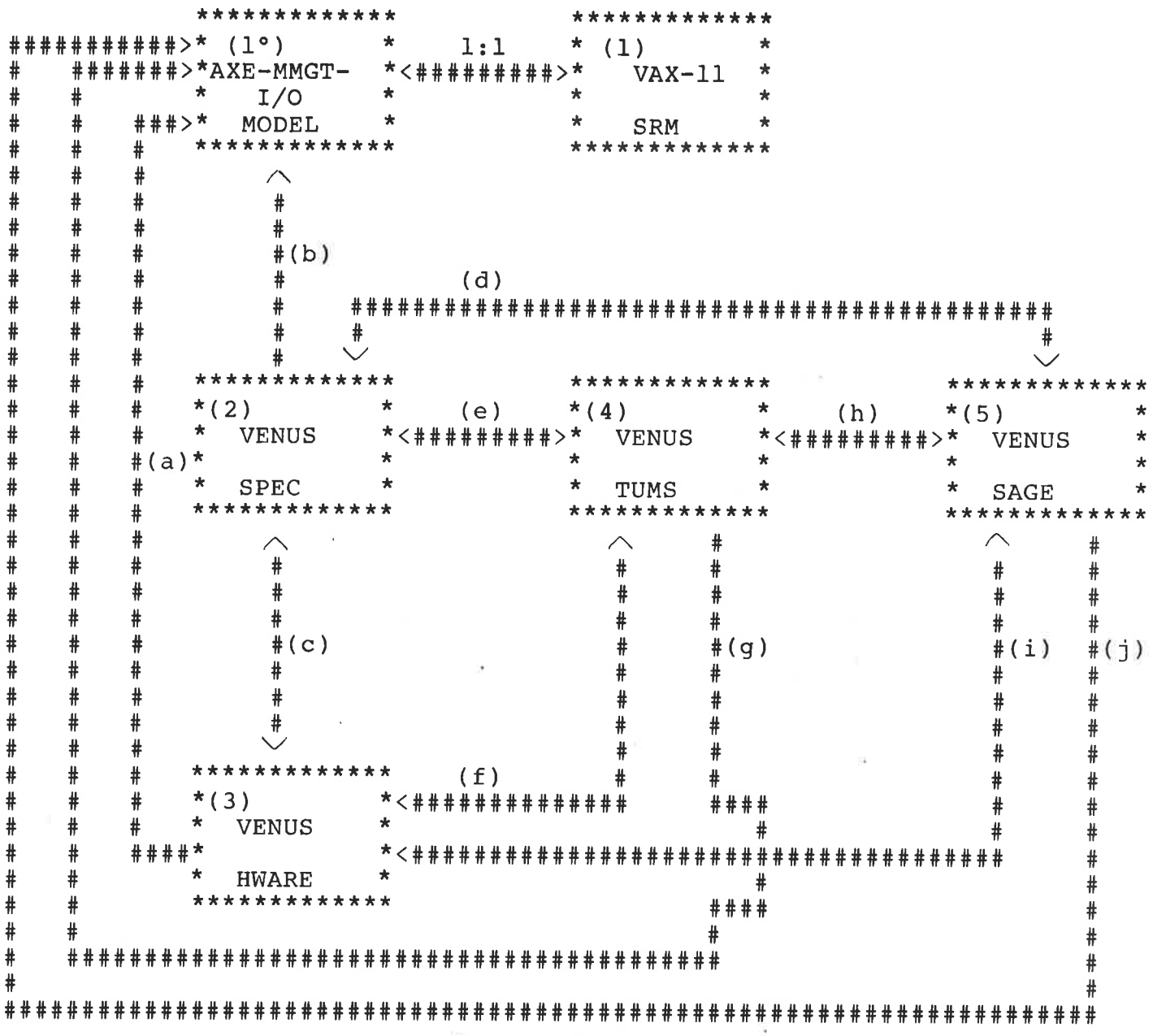


Figure 3.4 VENUS Validation Models

Expanded to include the AXE-MMGT-I/O Model of the VAX-11 architecture
(See notes on next page)

Notes for Figure 3.4

(a), (b), (c) as in Figure 3.2; however, the VAX-11 SRM model is replaced by AXE-MMGT-I/O model.

(d) 1:1 correspondence between VENUS SPEC and VENUS SAGE

(e) 1:1 correspondence between VENUS SPEC and VENUS TUMS.

(f) 1:1 correspondence between VENUS HWARE and Venus TUMS.

(g) VENUS TUMS model is a superset of the AXE-MMGT-I/O (i.e., "VAXness" of the TUMS model).

(h) 1:1 correspondence between VENUS TUMS and SAGE models.

(i) 1:1 correspondence between VENUS HWARE and VENUS SAGE.

(j) VENUS SAGE model is a superset of the AXE-MMGT-I/O (i.e., "VAXness" of the SAGE model).

3. Technology Evaluation

Concurrent with the above two stages, the Technology Group has been evaluating the various technological innovations that are under consideration for use in VENUS. This involves generating specifications, working with vendors to meet those specifications, and collecting the information on which the Program can base its decisions on which technologies to use and what tradeoffs to make. The most extensive evaluation procedure is that for the MCAs, discussed below.

The engineering and evaluation effort in MCA technology lies in three principal areas: development of software design tools, verification of the hardware design, and characterization and qualification of the finished parts.

The various steps in the creation of an MCA use many of the design, layout and testing tools discussed in the next section. The most important new tool in layout is MCACUT, the MCA version of the Merlin placement optimization system. This

uses a cutline approach that minimizes the number of nets crossing an imposed boundary by swapping equivalent entities; these entities may be complete cells, equivalent functions within cells, equivalent gates within functions, and equivalent pins within gates. Other parts of the project include enhancements to the IDEA circuit routing system, programs for creating and checking the artwork data base that serves as the input for making the IC mask, and programs for manipulating and analyzing test patterns.

The hardware part of the project includes determining those circuit parameters that predict operational performance of the chips, to verify that the various circuit elements implemented on a chip function correctly - both in theory through circuit simulation and in practice through evaluation and test verification - and to determine worst-case conditions that may be applied to automatic test hardware to support verification. The hardware development group also provides the necessary application support to the VENUS design team and serves as the technical interface to Motorola.

Completing the development strategy is a complete characterization of the test chips, followed by a qualification procedure that includes correlation among test systems, compliance with specifications, verification of the burn-in procedure, verification of performance of parts from several wafer lots, and thermal, mechanical, electrical and reliability testing.

Related functions are installation and organization of MCA manufacturing and test procedures in the Hudson facility and acquisition of parts.

4. Software Strategy

To ensure an operating system for VENUS in the hardware development time frame, the development strategy of the VMS Group in Spit Brook is to be heavily involved as an integral part of the VENUS team throughout the design of the system. A project leader for VENUS Software Integration is in place in the VENUS Program Office to assist them. The following strategy is based on the belief that there are no areas where the VMS executive lacks the mechanisms and structure to support the extensions required by VENUS; it is expected that enhancements to the current system will be sufficient for VENUS support.

a. Place product quality as the primary and over-riding goal above addition of new features.

b. VENUS is scheduled to ship three months after VMS V3B is submitted to SDC. VMS V3B will have all necessary VENUS support.

c. Schedule and implement VMS support for new interconnect adapters and peripherals as they become available. The general rule of thumb is that to support a given peripheral, firm specifications must be available one year before support is to be provided, and hardware must be available to VMS Development six months before submission of the VMS release to the SDC. However, complex devices such as HSC50 will require longer leadtime.

d. The present VENUS-VMS Project is restricted to activities in the executive layer of the software in three categories: booting and system initialization, system error handling, and IO. VENUS requirements that imply software development in the bundled products will be scheduled and implemented by the VMS Group in the normal phase review process for the appropriate VMS release. Even though the current project will not directly result in the implementation of bundled products, a major role of this project is to provide a communication and consulting path between VENUS and VMS. As VENUS product requirements are identified, this project will provide a focus to help ensure that schedule and technical needs are made known and satisfied within the constraints of the phase review process.

e. In the event that the VENUS team identifies the need for additional layered products, layered product requirements are defined by the VENUS Program, in which this project is a participant. The products themselves are defined and implemented using the phase review process, managed by the responsible development group. Conformance to the appropriate VMS standards and testing and integrating them into VMS is monitored by VMS program management. Refer to Appendix B for the current status of the layered products.

5. Prototype Stage

Engineering will build two and Manufacturing will build seven machines that implement a transition

from simulation to prototypes. These will run at full speed, will use all etched pc boards and backplanes, and will make use of the second-pass to third-pass MCA chips. The use of these machines is: one for CPU and Diagnostics Development, one for VMS Development, one for revision control ("Golden Machine"), one for IO Engineering (Configuration testing), one for FCC, DEC Standard, and Preliminary 102 testing, one for layered products testing, one for Field Service, and two for Manufacturing QV (kernels only at present).

6. Manufacturing Prototype Stage

Manufacturing will build fifteen more prototypes and will then update them to reflect the documentation when it is released. The goal is for these to be functionally identical to the Engineering prototypes. The Manufacturing prototypes will be built with Engineering support and maintained by Customer Service. These machines will utilize the revised versions of the pc boards and backplanes, and they will have the second- and then third-pass MCA chips. Disposition of these machines will be:

One for VMS,
One for DVT,
Four for DMT,
Four for Field Service training,
One for Final 102 testing,
One for Educational Services,
One for cluster testing, and
Two to be assigned by the Product Manager.

At this stage, System Engineering will use the prototypes to verify a limited number of system configurations. Since the initial prototype systems will be built and verified without released documents, we will set up an account for purchasing components and mechanical parts and to track actual costs instead of standardized costs.

7. Qualification

This final stage is for testing and verification (qualification) of many more system configurations utilizing CI, NI, Unibus devices, and Massbus devices.

3.2 DEVELOPMENT TOOLS

Being developed internally are a number of programs, many very large and complicated, to aid in hardware design. Although many of these tools are available thoughout the Corporation, most are being developed or enhanced specifically for the VENUS Program by the LSG CAD Group. These programs are generally referred to as CAD tools, for "computer aided design."

Basic Circuit Design

The fundamental CAD tool is SUDS, the Stanford University Design System. This is based on a sophisticated graphics editor that aids in the design and checking of logic circuits and drawing of circuit schematics. It also contains programs to create wirelist and plot files. The outputs of SUDS provide the inputs to CALDEC, IDEA, and most of the other software discussed below. The program also has facilities for interacting with the various intermediate products of the board and MCA layout procedures.

SAGE Simulator

From information provided by the SUDS wirelist file, SAGE simulates the hardware of individual MCAs and VENUS subsystems with the ability to inspect the interaction between individual gates in real time (although many times slower than actual gate speeds), to determine whether the logic actually does what it was designed to do. The whole CPU can also be simulated at the gate-level on a KL-10 using the multi-forking software developed by the LSCAD Group. The multi-forking software eliminates the address space limitations on 36-bit machines by simulating different boxes of the CPU in individual subordinate forks, each of which can use 256K words of available address space.

TUMS

The LSCAD Group will develop a TUMS model, at the register transfer level, of the VENUS CPU. The resulting model will run under TUMS to provide microcode debug capability and functional specification verification. The TUMS-AXE interface will be used to check the VAXness of VENUS architecture.

FUNCOM

This Functional Compression program automatically compresses gate-level descriptions of MCA chips in a SUDS database to equivalent boolean equations between

inputs and outputs. The address space required to store the gate-level description of an MCA chip is reduced by approximately 30% by a typical FUNCOM compression.

IDEA

This program is the successor to CALDEC. Like the earlier procedure, it uses SUDS outputs to lay out circuits, but it is more advanced and handles many more layers. Only IDEA has the capability needed for laying out MCA chips.

Placement Optimization System

These programs help the designer determine the optimal position of circuit elements from critical parameters supplied by the designer and known characteristics of the materials, including even the capacitance of metal runs. The original program (MINCUT) has been enhanced to handle MCAs (MCACUT) and PC boards (PINCUT). With the information provided by this software, the designer can go back to SUDS to enter real locations in the drawings and get more accurate metal area delay estimates.

MCA Verification

From the IDEA database, the TENART software checks design rules, verifies interconnections, and ultimately generates the CALMA database, which is the representation of the MCA design used by Motorola to create the chip.

Wirewrap

From wiring rules and from information about the special character of runs, their type and termination supplied by the user, the wirewrap package generates the pattern for wirewrapping a circuit board or backplane, including assigning twisted pair grounds and generating an NC tape.

Test Pattern Generation

The Teradyne LASAR program implements an algorithm that generates input and output test patterns for both simulators and hardware testers. This is used principally for MCA designs, which are generally sent to Digitest, but arrangements have been made to use the program in-house. This software is also used by the diagnostics team to evaluate test pattern coverage and isolation techniques.

Automatic Delay Calculation

Using the AUTODLY data structures, this program uses a different algorithm to calculate stable and unstable periods with respect to a system clock for all signals of the CPU. It relieves the engineers of the task of identifying by inspection the worst case path between two points. It also eliminates errors caused by incorrect identification of worst case paths.

3.3 PHASE REVIEW

The VENUS Program will follow the "Product Development Process" used by the Large System Group in Marlboro. This process details the entry and exit criteria for six phases, listed here with their completion dates.

Phase 0	Product Strategy and Requirements	Completed Q2/FY80
Phase 1	Product Definition and Planning	Completed Q2/FY83
Phase 2	Product Implementation	Q1/FY84
Phase 3	Product Qualification, Product Release, and Pilot Production	Q3/FY84
Phase 4	Product Continuation	
Phase 5	Product Retirement	

During Phase 1 the many detailed plans and specifications were created, the design reviews held, the necessary contracts signed, and the manufacturing plant selected. The culmination of this phase was the completion of the Product Business Plan and System Implementation Plan. These last two items, which constitute the subject of the Phase 1 Review, detail the course of the Program in Phase 2. During Phase 2 the Program will accomplish the following major tasks:

Renew commitments of Engineering, Manufacturing, Marketing and Customer Service to the revised Product Business Plan.

Hold technical reviews of the engineering design, manufacturing process, and service process.

Complete the detailed design, prototype test, and software internal tests; at the end of Phase 2, DMT and field testing will be ready to begin.

Run performance benchmarks and publish a performance report.

Make sure announcement criteria can be met. The principal criteria are that DMT be one-third done and there be a reliable second source for MCAs.

3.4 PROGRAM TRACKING AND MAJOR MILESTONES

Planning the development of the VENUS program involves fitting together schedules from various proups to insure that plans are complete and to highlight any holes or redundancies. The Project 2 program management software has been selected to assist in constructing an overall program schedule.

The first step in this process is for the supervisors or managers of the groups involved to document their plans using flowcharting techniques similar to PERT, specifying activity names, durations, and relationships to other activities. These inputs are entered into the Project 2 database and graphical networks are produced and returned to the user for updates or corrections.

After plans have been inputted and corrected, the next step is to assemble plans from the groups involved into an overall schedule. In addition, major program milestone events are identified for reporting purposes. This step is accomplished by holding meetings to clarify the dependencies, deliverables, and doneness criteria among groups.

The next step is to define the reports required, both at the program management level and within each of the groups. Project 2 has the capability of generating reports in several formats, including graphical outputs of the activity network, GANTT charts, working schedules, and planning schedules, to suit the needs of various users.

After an overall schedule has been created, a program management review is held to gain concurrence on the plan before it is published as the official base plan. Then schedules and reports are used to monitor key milestones and to understand critical path activities, with status changes made weekly.

Major Milestones

Throughout the course of the Program, there will be a number of particular events or milestones that must occur at specific times if the overall goals of the Program are to be met. Keeping track of the actual dates of these events as against the target dates

given here will provide a very good indication of whether the Program is on schedule and where any trouble may lie.

EBox SAGE Start	Complete
MBox SAGE Start	Complete
FBox SAGE Start	Complete
Test Vehicle 3 Start	Complete
EIM Boxes TUMS Models Complete	Complete
Proto 1 Power On (Ready for Modules)	Complete
EIMF Boxes in TUMS Run 5 Macroinstructions	Complete
2 SBIA Boards & Backpanel to Layout	9/82
CPU Logic Design Complete	9/82
IBox SAGE Start	9/82
Delay Analysis Tools Available	9/82
Start Console Test	9/82
Clock Board Available	11/82
EIMF Boxes in SAGE Run 5 Macroinstructions	11/82
EIMF Boxes in SAGE Run All Exception Test Cases	1/83
Total CPU Power On	2/83
Macro Hardcore Test Runs - Proto 1	3/83
Diagnostic Supervisor Runs	4/83
Start Testing VMS on VENUS	5/83
Start AXE	5/83
AXE (Slow) Runs 100K Cases	5/83
Preliminary 102 Testing Complete	6/83
All Technology Tests Complete	6/83
Start Layered Products Test	6/83
AXE Runs at Speed *	7/83
Preliminary FCC Testing Complete	8/83
UETP Runs Slow	9/83
Technology Released	10/83
VMS Critical Tests Run Slow	11/83
UETP Runs at Speed	11/83
VMS Critical Tests Run at Speed	12/83
VMS Ready for Field Test	1/84
Start DMT on 50 & 60 Hz Machines	1/84
DVT Complete	1/84
1/3 DMT Complete	2/84
FCC Testing Complete	2/84
Announcement	2/84
System Testing Complete	3/84
Start Build of First Production Machine	3/84
Start PMT	3/84
Release VMS 3.B to SDC	3/84
SPT Complete	4/84
Diagnostic Isolation Verified	4/84
Field Test Complete	5/84
DMT Complete	6/84
First Revenue Ship	6/84

* Speed defined between 72 and 90 nanoseconds

3.5 RISKS AND DEPENDENCIES

Following are some of the more critical risks, whose impact on the Program could be severe. In each case whatever actions can be taken to lessen the risk are indicated, and backup strategies are considered wherever appropriate.

Multi-Signal Layer, Controlled Impedance PC Boards and Backplanes

Boards and backplanes with multiple signal layers are absolutely necessary to provide sufficient component interconnectivity to allow the required component density. Such units are in general use, but no vendor can supply them in the quantity needed or at a suitable price. The risk here is in acquiring the know-how and capacity to manufacture them in-house. The Corporation is pursuing this path, and we will assist in any way we can in developing the necessary capabilities. There is sufficient outside capacity for the first year of VENUS shipments, but we must have in-house production from a volume plant by FY85. With this in mind, the MSL/CI Program Team is aggressively pursuing a plan to develop a pilot plant and then get into volume production. In a real sense there can be no backup for multilayer boards: the system as presently conceived is impossible without them. Backup for the backplane is to have as many layers as possible and take up the slack with twisted pairs; we are developing an interconnect model to determine exactly what is needed and how reliability is affected.

Transfer Cost

Eighty-one percent of Marlboro's transfer cost is in materials alone, and in many cases it is the high risk technology itself that is critical to meeting cost objectives: any alternative to MCAs and multilayer boards would be more expensive. Manufacturing is naturally pursuing all avenues for arranging the best possible terms for purchase of the needed materials, and is also investigating any savings that would result from bringing processes in-house rather than purchasing from vendors. Of particular importance is the establishment of volume in-house production of MSL boards, as the capacity is necessary not only to satisfy the need, but also to achieve the cost goal.

Software Synchronization

VENUS depends on VMS V3B's meeting its field test and SDC's submission dates as defined in the VMS V3B overall project plan (August 1982).

FCC Regulations

Current FCC rulings mandate testing, correction and documentation of all computer products.This new requirement pertains to radio frequency emissions from high speed switching in data processing equipment and electronic pollution of power lines resulting from ineffective or improper line filtering. This program will require a major effort for LSG. In preparation for the effective date of these regulations, the Technology Group has investigated the matter and issued a report outlining the kinds of programs required for both new and old products, their cost, and the cost and availability of test equipment and facilities. The report also lists current products that will have to be tested and corrected.

We shall handle the testing for the two cabinets unique to VENUS and insure that they satisfy the FCC requirements. In order to reduce the risks, several major steps have been taken, including: test equipment/qualified, personnel in place, test facilities established (shielded room, three-meter site), anechoic chamber under construction, FCC cabinet design completed, confidence level testing (KL-10 and 11/780 Repackaged) completed, analytical programs developed, and easy access to the free field (bubble) site insured. Moreover, we have worked with the 11/780 people concerning the optional Unibus and SBI expansion cabinets, for which they will now assume responsibility by repackaging into the new FCC VENUS/JUPITER cabinets. However, the principal problem area is the IO equipment, which is under the purview of the applicable development groups. Product Management has supplied the appropriate development group with a list of the options that we wish to support, and our IO group will work with the Engineering managers in the IO area to track possible solutions. Overall responsibility for ensuring that products meet FCC standards lies with the individual development groups: Distributed and Midrange Systems, Storage Systems, and Terminal and Small Systems have prepared their plans. It should be noted that there are legal issues that must be resolved, in particular how to test mixed and upgraded systems.

Product Safety, Acoustics and Telecommunications

Of concern are the product safety submittals to TUEV (German equivalent of UL). This is a new agency for DEC product submission and, as such, presents an unknown element. This risk is being reduced by the trial submission of subassemblies, with a high degree of success thus far. The acoustic area presents some

new difficulties in developing methods for reduction of the CPU fan noise. In this regard, special muffler designs are being formulated. The telecomm area is primarily the responsibility of the applicable VAX 11/780 comm group.

All of these areas, coupled with peripheral devices, present the highest risks, as they are under the control of the individual product lines, for insuring conformance to Product Safety, Acoustic, RFI/RMI, and Telecomm compliance.

Dependencies

Besides the major risk areas that could have such an adverse effect, the Program and its various parts are dependent for their fulfillment on the performance of many other people and groups throughout the Corporation. Here are some examples.

The design and layout of MCA chips, pc boards and modular backplanes are heavily dependent on the development of very sophisticated software, which in turn is heavily dependent on computer time and personnel to do the job. In addition to schedule risks, there are also risks in the processes themselves. For example, the representations of some complicated designs may be too cumbersome even to handle.

The peripheral strategy is especially dependent on the definition, funding, scheduling and meshing of projects from many other areas of the Corporation. These range from the Corporate Interconnect Strategy, whose failure could leave VENUS without cost-effective peripherals and create havoc for diagnostics, down to the availability of the UDA50.

3.6 TIME TO MARKET, SYSTEM CONFIGURATIONS, AND SUPPORTED PERIPHERALS

As explained in Section 1.1, the strategy is to go to market first with a system built on the CI Base, then go on to the smaller IDTC Base systems. FRS for CI-based systems is June, 1984. Figure 3.5 shows the volume shipping rate (in units per month) attainable by Manufacturing at the proposed Engineering schedule.

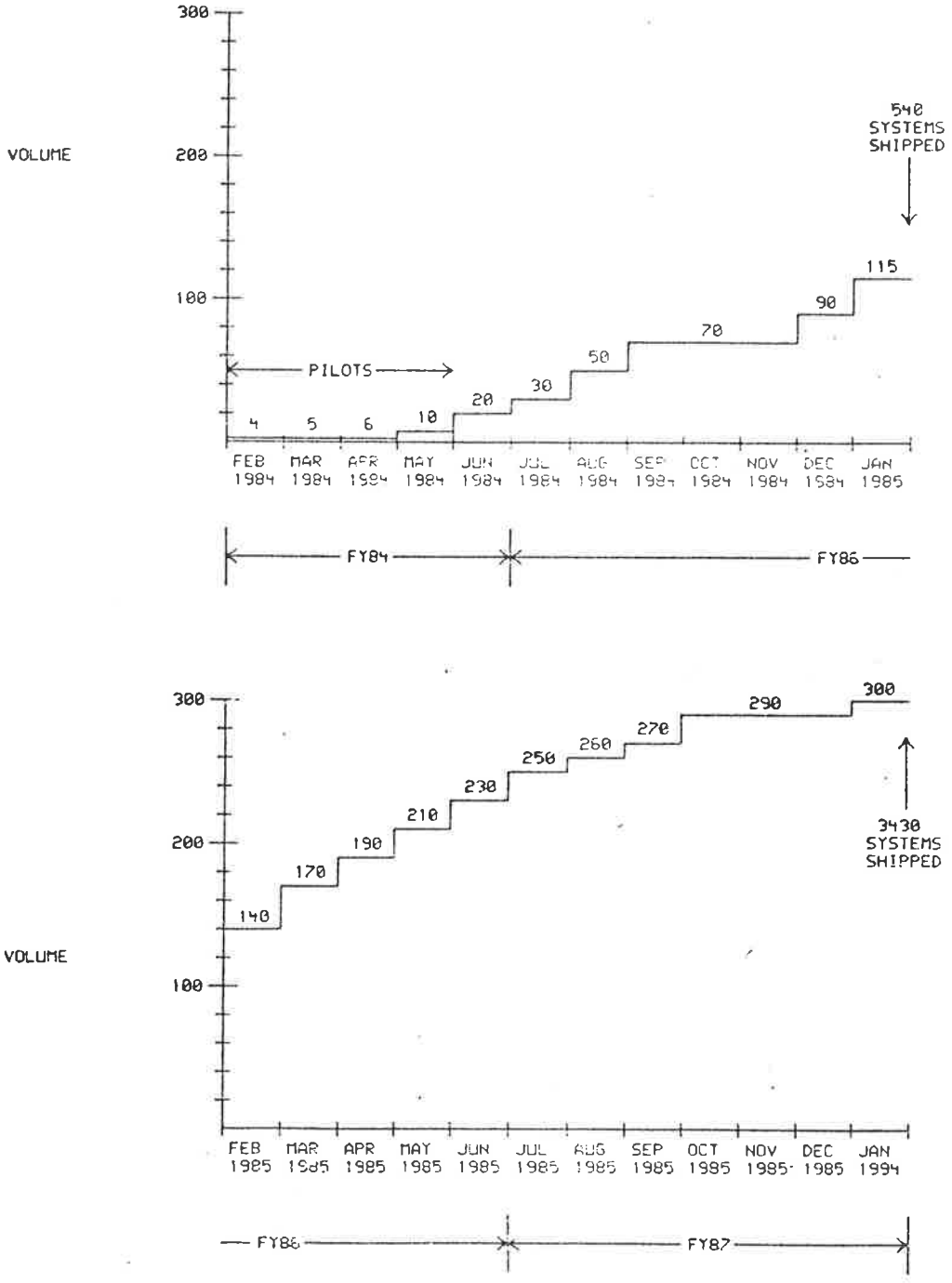


FIGURE 3.5 VENUS SYSTEM SHIPPING RATE

System Configurations

Both of the system kernels defined in Section 1.1 use a double width highboy CPU cabinet and an H9602xx Unibus-console cabinet; the CI Packaged System also requires lowboy cabinets for the HSC50 and RA81. Expansion possibilities in these and additional cabinets are as follows.

CPU cabinet
- At FRS
  - Floating point accelerator (FPA)
  - Additional memory to 32 MB in 4 MB increments
  - Additional Unibus adapter for extra IO
  - Serial line unit for remote diagnosis
  - Additional SBIA to add more adapters. (All adapters on second SBI must be mounted externally, i.e., in an SBI expansion cabinet)

Front End cabinet
- Contains 1 BA11-A mounting box for DMF32s, UNAs, DMR11s, DMP11s, DUP11s, DEUNAs, and so forth, 1 distribution panel, RL02 console load device, and optional stepdown transformer. A maximum of 48 communication and device control cables can be connected to the Unibus-Console Cabinet.

Additional standard 11/780-type Unibus expansion cabinets as needed

RA81 cabinet (H9642) - holds up to 3 RA81s

1 or 2 SBI expansion cabinets (at FRS + 6 months)
- Each cabinet can hold 4 adapters connected to the external SBI (a Massbus system requires 1 SBI expansion cabinet); available adapters are DW780, CI780, DR780, RH780

Optional Peripheral Equipment

During the first year after FRS, system configurations will be validated with additional options from among those listed here, and no others will be allowed. Options to be supported at FRS on new builds are indicated below:

Integration Site: Manufacturing FA&T (Shipped with System)

DMH32	UDA52	CI780	HSC50	DW780	SC008
DMF32	TA78	RL02	RA81	LA120	RA80
TU81					

Integration Site: Field

Dock Merge		Integrate at Fixed Charge		Integrate at Negotiated Price	
RA80	VT100	LPA11		TE16	TM/TU78
RA81	DMP11*	LA180	DN11	LP11	LPA11
RA60	DMR11*	LP25**	KMC11	LP14	TU77
UDA52*	DUP11*	LP26**	KMD11	RM03	LPR11
HSC50	DMF32*	RA80	DR11-W	RM05	
TA78	CI780*	RK07	DR780	RM80	
TU/TA81*	DW780*	RX02	DW780	RP07	
LA34	RH780*	TS11	CI780	RP06	
UNA*	DR780	DZ11	RH780		
LA38	SC008	DZ32	LN01		
LA120	DMH32				

* Options dock mergeable only when installed in backplane slots in the CPU cabinet or attached Unibus console or expansion cabinets.

** Dock mergeable only when being controlled by DMF32.

NOTE: IO devices listed under Dock Merge can also be Integrated at Fixed Charge or Negotiated Price. IO devices listed under Integrate at Fixed Charge can also be Integrated at Negotiated Price.

4 COST

The major cost categories that must be considered are the cost of developing the product, the cost of building it, and the life cycle cost.

4.1 DEVELOPMENT COST

Included in this category are all design expenses, plus the pre-FRS startup expense for Manufacturing, Hudson LSI, and Customer Service. Figures given in the tables on the next three pages are in thousands of dollars.

Hardware and Software Engineering

The hardware budget given on the next page includes material expenses to cover building six Engineering prototype systems, creating all diagnostic programs, releasing fifty-three MCA types, nineteen L modules and four backpanels to Manufacturing, and integrating all devices that we have committed to support. Also included are funds for VENUS's share of the FCC and MSL Programs, and for Manufacturing process development (assembly and test) as stipulated in the Manufacturing Product/Process Strategy. Following each line item is the name of the responsible manager. Note that the budget does not include funding for building the Manufacturing prototype systems. It is estimated that these will cost approximately $100K each, and we recommend that X95 manufacturing accounts be opened to capture these costs. Individual user groups must capitalize and depreciate their machines, as the Corporation will charge them off to the various cost centers over five years.

Base Plan Budget Charlie Williams

Group	FY83	FY84	FY85	FY86	Total
Technology	2462	1872	545		4,879
CAD	1200	200			1,400
Mass Storage (Memory)	154				154
Qualification	70	354	200	200	824
LSI A&T	1237	300			1,537
LS Computer Operations	3627	3848	2503		9,978
Engineering Services	1723	669	690		3,082
MPS Program	300				300
Mfg Module Test	50	500			550
Educational Services	150	200			350
Eng/Mfg ECO (cont.)		1000	2000		3,000
LVE	5227	6980	3615	1800	17,622
Total	16200	15923	9553	2000	$43,676K

Manufacturing Startup — Bob Murphy, John Grose

	FY80	FY81	FY82	FY83	FY84	Total
MFG* new prod. startup	127	922	1990	4577	4658	12,274
MR capital and tooling			59	1908	4933	6,900
MO new product startup			60	88	108	257
MO capital and tooling				1700		1,700
Total	127	922	2109	8273	9701	$21,131K

*Includes MR, EBB, BT, KA, and GN

Hudson Startup — Ken Brabitz

	Past	FY82	FY83	FY84	FY85	Total
E97 New process						
Manpower	197	580	295			1,072
Contract	50	100				150
Material	214	305	152			671
E96 Plant funding						
Manpower	129	304	514	396	135	1,478
Material		312	504	336	119	1,271
Masks	39	96	189	108	48	480
CAD		14	37	24	10	85
Tester hardware	17	36	18	6		77
Qualification	23	74	14			111
Software	20	60	16			96
E69 New product startup		32	18			50
Capital equipment	815	412	800	65	500	2,592
Total	1464	2255	2635	961	818	$8,133K
Old Budget	2026	1557	2150	744	8890	$7,367K
	<562>	698	485	217	<72>	$ 766K

Customer Service Startup Reg Burgess

	FY83	FY84	Total
CS System Engineering			
ME Group	306	408	714
Spear Group	51	102	153
ESD&P	406	406	812
Training		290	290
Capital			
MEG Proto		272	272
ESD&P Proto		272	272
Software ME Group	51	102	153
Total	814	1852	$2666K

4.2 MANUFACTURING COST

Here we consider the actual cost of producing an individual system. Figures are in dollars, estimated for the 1000th Basic System with the dollar valued at time of production. Also given is a detailed breakdown of the processor based on these vendor costs for shipments in FY85:

MCA	33.20	8-signal-layer module	200
1K RAM	4.00	Memory register file chip	10
4K RAM	8.00	A bus interface chip	21.60
256K MOS chip	21.58		

The above figures are actual vendor quotes, and they can be expected to fluctuate depending on volume, yield, and the general economic situation. As has already been pointed out in Section 3.5, at steady state 81% of the cost of the CPU kernel is materials, and Manufacturing is investigating every possibility of savings, both in purchasing and in developing in-house capabilities. The projected MSL cost is expected to decrease considerably in FY85 with in-house production from a volume plant. Note that the following costs are contingent on Diagnostic chip isolation.

Processor

Double width cabinet with power	$ 7,485
Battery backup	769
I/E box modules (11)	10,183
M box modules (3)	3,359
Console module (1), LA120	1,614
CPU/memory/A bus backplanes	2,104
IO backplane	827
Memory bus terminator	377
A bus & SBI terminator	376
FPA Terminator	370
1 SBI adapter	1,614
Assembly (46 hours)	2,841
CPU test (21 hours)	1,701
Total	$33,620

Unibus-console Kernel

H9602-xx cabinet	663
1 BA11-AL/AM mounting box	1,323
2 DD11-DK backplanes, 1 DD-11-CK, 1 DDU-11-CK	600
2 M9202 jumper cards	69
20 G727 continuity cards	63
1 DMF32-C Combo with distribution panel	1,206
1 RL02 disk (RLV22-AK)	1,269
Assembly (13 hours)	819
Test (1 hour)	81
1 M9302	32
1 M9403	62
1 M9400-YB	22
Total	$ 6,209

CPU Kernel

Processor	$33,620
4 MB memory	4,491
1 DW780xx Unibus adapter	1,206
1 Unibus-console kernel	6,209
Cables	80
Packaging	150
Total	$44,550

CI Base

CPU Kernel	$44,550
1 CI780 adapter	2,455
1 HSC50 controller	9,800
SC008	800
3 RA81 disk	15,286
1 TA78 tape	15,265
Total	$88,136

IDTC Base

CPU Kernel		$44,550
1 DW780-UDA50 disk-tape controller		2,356
1 LCGCR tape (TU81) drive & controller		6,400
1 RA81 disk		5,082
1 Pinon disk (RA60)	3,500	
Total	$56,806	$58,388

Optional Equipment

FPA	$3,315
4 MB memory array module	4,491
Pinon disk (RA60)	3,500
LCGCR tape (TU81)	6,400
LP26 line printer	4,494
SBI adapter	1,614
H9602-HA/HB SBI expansion cabinet	1,828
Stepdown transformer	600
Unibus expansion cabinet (less BA11 drawer)	1,300

4.3 LIFE CYCLE COST

A fundamental concept underlying the program to create the VENUS system is to minimize the total cost of that system over its entire life while at the same time promoting the greatest possible customer satisfaction. With this objective in mind, in August, 1979 Win Hindle formed a VENUS System Life Cycle Cost Task Force (Ulf Fagerquist, chairman; Walter Manter and Dave Thorpe, members). The Task Force is studying the total life cost of engineering, manufacturing, installation, warranty and service for VENUS systems with a view toward achieving these three objectives:

a) To develop methods and define parameters for establishing and forecasting levels of customer expectation and satisfaction.

b) To develop methods for minimizing the total cost and maximizing customer satisfaction for the VENUS system, especially methods that do not require additional expenditures.

c) To develop an integrated financial model as a tool for evaluating the efficacy of the methods developed in b).

The results of the efforts outlined above will of course be general in nature and applicable to any project. For the immediate situation, the key objective of the task force is to set the direction and give proper guidelines for the VENUS Program. These guidelines should give visibility to the need for committment to Corporate-wide processes for the planning, integration, and implementation of the Program across all functions: sales, product lines, services, manufacturing, engineering, etc.

In conjunction with the Task Force, VENUS Program leaders have already generated a list of desired alternatives related to life cycle cost. Dates for resolution of these alternatives have been set ranging from 3/80 to 12/81 depending on priorities and needs. Some of the more important alternatives and the dates that they were resolved are these.

HPP vs conventional mechanical packaging (conventional packaging selected)	3/80
Sockets for RAMs (will be used)	7/80
Sockets for MCAs (will be used)	12/80
Level of dock merge	6/81
Burn-in of components	6/81
Provide module level specifications	6/81
Improve Field Service reports	12/81

5 SYSTEM REALIZATION STRATEGIES

It is one thing to define a logical system and even to develop it into a physical entity, but then the result must be made a reality - it must be manufactured as a marketable, maintainable product. Following are the strategies for accomplishing this objective.

5.1 MANUFACTURING STRATEGY

Manufacturing involves special considerations for the components. The MCA build process developed by Motorola has been purchased by the Corporation and transferred into our Hudson facility. The MCAs will be tested by both Motorola and LSI Central Incoming Test using the D-LASAR program. Incoming 1K and 4K RAMS will also be tested at LSI. Remaining ECL components are expected to be high reliability parts.

The modules for VENUS will be built, tested up to QV level, then integrated in volume with backplanes, power supplies, cabinet, and memory to form a CPU kernel. This kernel is intended to be POM (Point of Manufacture). It is expected that there will be two categories of system, one that is POM out of the volume area, including some custom configuration; and one requiring full system spec testing. These two categories are referred to as preconfigured systems and complex or a la carte systems.

Preconfigured systems will be assembled using off-the-shelf options from the stockroom, and it is expected that time to ship from receipt of customer order will be one week. The stock kept on hand will be determined by marketing forecasts.

Based on marketing forecasts, Manufacturing will build a number of preconfigured systems of various types documented and verified by Engineering. Then upon receipt of a customer order, the appropriate

system will be taken directly from finished goods stock, with possible add-on of perhaps one or two dock-mergeable custom options.

Complex systems will be assembled individually from finished goods stock upon receipt of customer order. The time required will be four weeks, and it is expected that only these systems will carry current FA&T costs.

Marlboro has been selected as the prime plant for the introduction of the VENUS system. Bob Murphy, the System Manufacturing Program Manager, will be addressing all issues relating to VENUS manufacturing.

5.2 POINT OF MANUFACTURE (POM)

Both Engineering and Manufacturing feel that considerable savings in FA&T costs can result from having as much of the system as possible be POM. To this end we will do the following:

We will make certain all of the equipment we design is POM. At FRS the basic CPU kernel produced by Manufacturing for all systems will be the CPU cluster plus 4 MB of memory. This is appropriate for all systems that will be delivered in the early stages, and Manufacturing is prepared to create a larger kernel should that become necessary. For final testing each kernel will include an FPA, but it will then be removed, and both it and the kernel will be stocked separately as POM options.

We have already determined which peripherals will be supported at FRS and which at FRS + 12 months; all of these, listed at the end of Section 3.6, will be POM. POM is now a Corporate goal for all new products, and we will attempt to make maximum use of such new products. Furthermore, wherever feasible, we will do our best to influence the individual development groups to qualify whatever of their current products that we may decide to support in the future.

Manufacturing is currently conducting an analysis of its procedures with a view toward making whatever modifications are necessary for POM. Areas particularly affected are the process, material and capitalization plans.

For the success of POM, Manufacturing is dependent on Qualification Engineering and Customer Service.

Qualifying a product for POM relies principally on the various maturity tests and the many qualification tests outlined in the next section. Jointly with Customer Service, Manufacturing will conduct sample audits of specific products during installation, and will establish a formal feedback procedure for information on whether dock-merged systems are living up to their expectations in the field.

We will define a reasonable number of preconfigured systems of various sizes to allow the greatest degree of POM, consistent with reasonable cost and flexibility in tailoring individual systems to customers' needs. For this purpose we will maintain strict revision control in order to know the status of all elements at all times.

If this endeavor is successful, peripheral controllers and extra memory array boards can be tested on a single CPU kernel kept right on the test floor, rather than needing to be tested with the particular options that will appear in a final customer system. This will of course eliminate a great deal of handling. The various options will be kept on the shelf, and final asssembly of a customer system can be accomplished by merging a CPU kernel with the FPA, extra memory, peripherals, and the software package.

Even for systems including devices that are not POM, there is no need to assemble the individual customer system for final test. Instead the FA&T area will have several option test stations available on the test floor. Then for a special system, the non POM items can be tested on these stations.

5.3 QUALIFICATION PLAN

This plan defines the steps required to ensure that VENUS is a qualified product. To be qualified the system must:

Adhere to Engineering functional and performance specifications.

Achieve product cost goals.

Achieve MTBF and MTTR goals.

Undergo a formal DMT and PMT to prove that the system lives up to defined RAMP goals.

Conform to national and international regulations as required in DEC Standards 052, 060, 103, 104, 105, and 119.

Obtain approval certification from UL, CSA, VDE, and FCC.

Endure environmental changes as required in DEC Standard 102.

Qualification approaches the product from a system level to prove that this system can perform the functions previous systems have and to build confidence in areas of risk. A risk area is any as yet unproven functionality or technology. To reduce exposure to risk, vulnerable areas will be identified and provisions made to test them. A heavy emphasis will be placed on ensuring that all system RAMP features are achieved.

Testing procedures fall into two general categories, system qualification and product performance. The schedule for these tasks is determined principally by the schedule for the Program as a whole.

System Qualification Tests

These are tests to confirm that VENUS lives up to its design specifications in the areas of sensitivity to various conditions, conformance to DEC standards, functionality of various procedures and features, and characteristics of the overall system. Tests are performed in the following categories.

Sensitivity of the system to margins in voltage, temperature, humidity, and clock rate.

Conformance of electrical characteristics to international regulations, DEC Standards 102.7 (particularly EMI/RFI), 122 and 123, and FCC requirements.

Conformance of mechanical characteristics to international regulations and DEC Standards 102 and 119.

Sensitivity of environmental and power sensors.

Verification of performance under voltage margins.

Verification of all power up/down sequences.

Verification of initialization and configuration routines utilized to prepare the system for bootstrapping.

Verification of the bootstrap program via all load paths.

Verification of software support of the hardware (i.e. functionality of the operating system).

Verification of the orderly shutdown of the operating system.

Verification of the diagnostics used in the manufacture of the system, other than those associated with special test equipment, which will be verified by Manufacturing.

Verification that the diagnostics provide the tools necessary to maintain the system.

Verification of system RAMP features.

Determination of the sensitivity of the hardware and software to variations in system configuration.

Determination of the reliability of the hardware and software, especially RAMP features, through the design maturity test (to measure MTBF) and a software load test.

Product Performance Tests

Hardware and software benchmarks will be run to measure the performance of the system against existing Digital computers and those of certain competition.

5.4 DIAGNOSTIC STRATEGY

The Diagnostic Project for VENUS is seen as a comprehensive effort designed to serve the needs of Engineering during design verification and prototype debug, Manufacturing from start up through volume production, and Customer Service to meet their repair and maintenance cost goals. The effort includes consultation with the various groups to set realistic and achievable RAMP goals; participation in planning implementations which achieve those goals; design, implementation, debug and complete documentation of new code; and contracting with other groups, where appropriate, for modifications to and verification of existing VAX diagnostic code.

The VAX diagnostic architecture is based on a hierarchical approach to the problem of testing and diagnosing problems. An intelligent console is used as the core of the diagnostic operation, utilizing its access to the basic controls of the main CPU. Functions such as loading control store RAMs and controlling clock cycles are available to programs residing in the console computer.

The lowest level of diagnostic hierarchy is the CPU microdiagnostic, consisting of the control store which runs tests and the console which monitors results. The tests in the microdiagnostic sequence are ordered in such a way as to create a gradual increase in the amount of tested logic. This "bootstrapping order" simplifies the problem of locating a failure, which is usually in the newly-included logic under test.

The next hierarchical level, provided by the CPU cluster exerciser, is a "behavioral test" of the complete CPU, memory, and adapters. A major portion of the exerciser is concerned with verifying that a sample of the VAX instructions and other functions such as memory management behave as described in the VAX System Reference Manual. Because of the vastness of the VAX architecture, these tests are not exhaustive, but they do serve as a confidence check on whether the right microcode and other RAM data were installed correctly and on whether the hardware portions tested by microdiagnostics function as a "whole" VAX.

The VAX peripheral diagnostics constitute the next level -- or actually two levels in that they are often referred to as "level two's" and "level three's." A level two program is a functional or behavioral test which runs in VMS user mode and contains an exerciser routine and often a formatter, as in the case of discs. The level three program is a repair diagnostic which pinpoints failing replaceable units in addition to responding to functional failure symptoms.

A key element of the VAX peripheral diagnostics is the diagnostic supervisor, a package of standards, macros, and utility routines which form the heart of all VAX level three programs. Its main purpose is to mask the attachment of a peripheral to a VAX CPU and differences among CPUs. The supervisor provides a "stand-alone" diagnostic operating environment, and the VAX diagnostics which utilize it are transportable throughout the entire VAX family.

At the highest level of the VAX diagnostic set is the system exerciser. This exerciser, which runs under VMS and uses portions of the level two programs for all the peripherals, is designed to be a confidence test of a complete VAX system.

In addition to the actual diagnostics and test programs, the VENUS Diagnostic Product includes extensive support software. This software is needed by LVD to generate, load, run and check out diagnostics; by Engineering to debug early hardware and microcode; by VMS software to support the runtime system; by Manufacturing to support the use of their APT system; and by Customer Service to support remote diagnosis of customer machines.

Diagnostic Goals

The major goals of the VENUS repair level diagnostics may be summarized as follows:

DETECTION of more than 99% of all solid faults in the CPU Cluster.

Correct ISOLATION of those faults to the failing module in better than 95% of all instances.

Correct ISOLATION of those faults to a set of failing components to the degree that hardware visibility features permit. (It is highly desirable to achieve isolation to three or fewer components. LVD will examine each hardware module and assess the degree of component isolation achievable with the design. The Diagnostic Functional Specification for each diagnostic will address the degree of isolation thought possible.)

NO FAULT runtime of less than twenty minutes for the CPU.

Time to ISOLATE a solid fault (to the failing module) of no more than two minutes following the detection of a fault.

SUPPLYING a console software package which will support both stand-alone diagnosis and normal system (VMS) operation.

Dependencies

A large scale system development effort such as VENUS is by nature a highly interdependent environment. Large VAX Diagnostics is dependent on the following groups for the following items:

Hardware Engineering to keep their schedules and provide the diagnostic logic necessary to carry out this plan.

Hardware Engineering to provide timely specifications and information necessary for LVD to design and code the VENUS diagnostics.

Hardware Engineering and Marlboro Operations to provide various computer resources.

Large Systems Group Management for funding in a timely enough manner to allow hiring and training of the necessary new personnel.

The VAX Diagnostic Supervisor Group to keep their schedule and provide the VENUS version of the DS.

The VAX Mass Storage Diagnostic Group in Maynard to keep their schedule and provide qualified diagnostics for the peripherals specified in the VENUS IO Plan for the SBI-based FRS system.

The VAX Comm and Unit Record Diagnostic Group in Merimack to keep their schedule and provide qualified diagnostics for the FRS peripherals specified in the VENUS IO Plan.

5.5 CUSTOMER SERVICE PLAN

The Customer Service Plan defines a set of installation and maintenance commitments based on an established maintenance philosophy. These commitments are listed in Section 1.1; the philosophy supporting them is given here, followed by a short discussion of the functionality of some of the major RAMP features.

Maintenance Philosophy

The general approach to corrective maintenance is that symptoms of malfunctions will be investigated first at the operating system level (it is in fact the first level maintenance tool). Information pertaining to the malfunction should guide maintenance activity to a particular area of the system for further diagnosis. This general or specific area will then be diagnosed, in as few modes as possible, until the malfunction is resolved to a field replaceable unit (FRU).

Materials

We will stock at least one full set of modules at the branch level, and this will be backed up by safety stock at the Corporate level. With RAM and MCA replacement a reality, the branch will also stock individual ICs and will be less likely to increase the number of modules as the population expands. Our goal is to ensure 99% reliable operation of spare modules. To reach this goal we will test them in-house in either standalone mode (new modules) or under the operating system (repaired/reworked modules).

Manpower

We plan a high degree of specialization at the branch level and expect to take advantage of 11/780 personnel during the startup phase. General system trouble-shooters will be at the DDC and in the Branch, District, Regional, and Corporate Support Groups.

Training

In conjunction with manpower recruitment we will establish both unit and subsystem specialist courses as well as system level troubleshooting courses. The expected length of the CPU-cluster specialist course is three weeks, and the system level or support course will take about five weeks.

Technical Documentation

Technical Documentation will support both the educational effort and the field maintenance effort. We expect to provide documentation in the form of print sets, maintenance manuals and procedures, site prep/installation/acceptance guides, microcode flow charts, IPBs, and theory of operation.

Remote Diagnosis

The current strategy for utilizing RD is to have the customer call the Digital Diagnostic Center in Colorado for initial diagnosis of a malfunction. The DDC will utilize a host computer to carry out the diagnosis of many systems in parallel. Once the DDC has determined that a failure exists and has isolated it, the local branch specialist will be dispatched with the proper set of FRUs to correct the problem. Software Service plans to utilize remote connection capabilities almost exclusively.

Major RAMP Design Functionality

System Error Detection, Logging, and Recovery

The operating system software, which includes certain system-critical console software processes (and possibly system firmware) will take a predefined course of action upon detection of any hardware or software error. This specifically includes recording various amounts of data, which will be utilized for immediate recovery processes. This data will also be analyzed by Customer Service with the new System Error Analyzer, SPEAR, for maintenance activities.

Hardware Error Detection Logic

All system components are being designed, where possible, to include hardware error detection or correction (not necessarily ECC) on all buses, internal data paths, RAMs and MOS memory. The current assumption is that error checking will cover at least 40% of the expected hardware failures. This error checking, along with the gathering of pertinent hardware status by firmware, the console or the operating system, should enable the system to isolate intermittent errors to one or two modules in the CPU cluster. For other parts of the system, isolation should be at least to the unit (controller or peripheral).

Remote Diagnostic Link

The console design, in conjunction with the console software and operating system software, will support a remote diagnostic link. This will be used for both standalone diagnosis and system level control and monitoring.

Environmental Monitoring

The console will monitor the thermodynamic and power systems in such a manner as to provide operator notification of most typical temperature problems. The power system will be monitored to the extent needed to isolate the cause of a malfunction to the power control or individual regulator.

6 FUNCTIONAL CHARACTERISTICS

Having explained what the system is and how we intend to develop it, let us now consider in somewhat greater detail just how it is expected to work.

6.1 CPU CLUSTER

An introduction to the functionality of the central part of the system has already been given in Section 2.1. The internal logic of the processor - ALU, data paths, RAMs, buses - is organized in terms of long-words of thirty-two bits, with transfers to and from memory in blocks of sixteen bytes (four longwords). From the program point of view the fundamental orientation of the machine is toward bytes, but with complete capacity for handling words, longwords, etc with arbitrary byte boundaries, although operation is most efficient when operands are kept aligned with the memory byte blocks.

I, E and F Boxes

The 8K x 84 writable control store is in the E box; each of the other boxes has a small control store with special microcode for its own operations.

The I box continuously prefetches the instruction byte stream and stores it ahead in an 8-byte instruction buffer, eliminating most of the performance penalty imposed by instructions crossing physical memory boundaries. Op codes and specifiers are decoded from the instruction buffer. For initiating instruction execution in the E box, the op code selects a location in a dispatch RAM; there are two of these, for native and compatibility modes (i.e. for the VAX and PDP-11 instruction sets respectively). The I box also contains an ALU and a copy of the general purpose registers (GPRs) for calculating addresses.

The E box contains the major part of the microcode, namely that which handles the execution of the instructions. The unit is based on a 32-bit binary/BCD ALU and a 64-bit left shifter and data packer/unpacker, both of which receive input from a pair of multiplexers. Available inputs are the operand bus, a pair of 256 x 32 scratch pads (each of which contains a copy of the GPRs), the Q register associated with the ALU for multiplication and division, and the W register, which receives input from either the ALU or the shifter. Besides instruction execution, the E box also handles machine initialization, interrupt processing, memory management, fault and error processing, and console support.

The F box is an option to the VENUS processor which, when present, will support F, D, G, and H-format instructions and will execute floating point instructions in the instruction stream. It is microprogrammed, but its speed and power stem mainly from a 32-bit datapath with specialized hardware for performing additions, multiplications, and divisions. Its cycle time is half of the base machine cycle time, namely 36.36 ns.

The actual operand fetching and storing is done by the I box, and the storing of the result is done under control of the E box. However, when the floating point accelerator is present, the E box no longer attempts to execute the floating point instructions, instead assisting the F box by providing addresses and taking care of exceptional conditions.

In addition to speeding up floating point instructions, the F box will also accelerate certain integer arithmetic operations. For example, integer multiplications and their extended versions for multiple precision arithmetic will take advantage of the high speed hardware in the F box.

It also contains special hardware for handling overflow and underflow conditions. The VAX architecture now requires that these cases be treated as faults, which means that no data is modified before the exception handler is entered.

As part of its error checking, the F box runs self test diagnostics when it is not involved with floating point instructions. This checking allows it to verify the correct operation of combinatorial logic in a cost effective manner without slowing down floating point operations.

Memory Subsystem

This subsystem includes the storage array boards (4 MB per board) and the M box, which contains not only all of the control, transfer and error logic for the storage array, but the data cache as well. The basic storage unit is a block of four 39-bit words, each containing four data bytes and a 7-bit error correction code.

The cache is 2-way set associative utilizing a writeback storage algorithm. The block size is sixteen bytes (each with a parity bit) and the total storage capacity is 16K bytes. Associated with each of the 256 blocks are valid and written bits and a tag that identifies the block. Replacement is on the basis of the least recently used entry, and write allocation is by block to simplify IO reading. Special logic is included for byte write, significantly decreasing storage access requirements. When memory data containing a corrected error is placed in the cache, the written bit is turned on to force eventual rewrite of the memory location, thus reducing the probability of a double error.

The control logic includes a translation buffer or page table for translating virtual into physical addresses. The buffer contains 512 entries each for system space and process space.

Console

The console is actually a microcomputer-based subsystem. It monitors environmental and power supply conditions, serves as the VMS operating system terminal, and provides an assortment of diagnostic functions. Via the I bus the microprocessor initializes and bootstraps the system and implements such functions as examine, deposit, start, halt. The serial diagnostic bus is used to initialize various diagnostic operations and monitor backplane signals and other error and diagnostic conditions. Besides the microprocessor and its associated logic, the hardware includes a PROM for the bootstrap code, a control RAM for the console microcode; controllers for the console load device, console terminal, and remote diagnostic link; and the environmental and power monitors.

6.2 PERIPHERALS

Hardware in the area of peripherals includes many already existing products or committed projects whose

functionality is already known or defined elsewhere. We therefore concentrate here on the adapters, controllers and devices whose development is specifically for VENUS.

A Bus Adapters

The SBI adapter, implemented with TTL MSI and 10K ECL logic, interfaces the A bus to the SBI. It provides all of the SBI functions necessary for handling CI, Unibus, Massbus, and other devices available on the 11/780 SBI, except that it is not intended to serve as a direct connection to other processors or memory. The hardware provides protocol, timing and termination for the SBI, and includes registers and data assembly facilities for transfers in both directions.

Mass Storage

In addition to certain enhancements to already available controllers, the VENUS Program expects to make use of the following two controllers whose functional character has been determined. The mass storage devices for these controllers are covered in Section 2.3.

HSC50 - This intelligent controller contains six subcontrollers for disk and tape systems. It is based on a microprocessor that optimizes the data buffering, continued IO overlapped with error handling, and overlapped or ordered seeks. It also provides many RAMP features, such as comprehensive error detection and recovery, bad-block revectoring, online volume backup, self-contained diagnostics, online drive repair, a remote diagnostic connection, and support for logical redundancies.

UDA50 - This intelligent controller contains four subcontrollers just for disks. It has the basic features of the HSC50 for low cost, medium performance systems.

6.3 SOFTWARE

At present the only system software functionalities identified as needed for VENUS are in the executive layer. These include support of the processor, IO adapters, RAMP features and console; bootstrapping and initialization; and error handling procedures. The VMS project for VENUS will do the following:

Modify the VMS software bootstrap procedure to configure VENUS IO adapters, IO address space, and memory address space.

Implement loadable VENUS-specific code for handling run-time processor dependencies. This code will include the capability for handling machine check errors, for saving and restoring nonarchitectural processor registers on power fail/recovery and bugcheck, and for handling errors from IO adapters.

Modify SYSGEN for VENUS specific testing of IO configuration.

Implement a driver for the console load device.

Enhance the error reporting mechanism to allow logging of errors detected by the console.

Support booting from any new devices required by VENUS, such as a system disk.

Support two SBIs.

Integrate all VENUS changes into the VMS master sources and system build procedure.

Layered Products

The VMS Group does not directly handle unbundled products, but VMS management is responsible for setting system goals and providing the overall system plan. Hence the Group would be involved in any projects recommended for VENUS, which might include enhancements to the FORTRAN compiler for better optimization, additional languages such as ADA, and support of additional communication ports to other vendors. Of course most of the required layered products are already under development, as indicated in Appendix B. Basically these products fall into five categories.

LANGUAGE PROCESSORS: By VMS Release 3 the following languages had been implemented with native mode compiler and execution: FORTRAN; COBOL; BASIC; PL/I; PASCAL; BLISS; DIBOL, which is important in the COEM market; and C, the system implementation language developed by Bell Labs for UNIX. Also VAX-11 DSM is available as a native mode interpreter, and CORAL-66 as a compatibility mode compiler with native mode execution. New languages in the planning or development stages are ADA and APL in a common implementation with the DECsystem-10/20. In most

cases, development is implemented to the latest ANSI or "de facto" standard plus enhancements that improve competitiveness. New releases will generally use new features of the VMS release and will therefore be synchronized to it, but this is not an actual goal. VAX-11 BASIC will be continually emphasized as the vehicle for RSTS/E users to achieve compatibility with BASIC-PLUS and BASIC-PLUS-2.

COMMUNICATION PRODUCTS: With the release of VMS Version 3, DECnet was bundled with VMS for single node applications. The purchase of a DECnet license enables multi-node network configuration. At VENUS FRS, DECnet/VAX will contain support for CI, NI, and X.25 communication links in addition to the existing synchronous links. Communications to non-DEC CPU's is possible with MUX200 (CDC), 2780/3780 and 3271 (IBM) Protocol Emulators. At VENUS FRS, connection to an IBM SNA network will be possible using a gateway precedent.

DATA MANAGEMENT: RMS (sequential, relative and ISAM file management) is bundled with VMS and interfaces with DECnet for remote file access. CODASYL compliant Database Management is provided with VAX-11 DBMS. Interactive inquiry, report writing, and distributed data base access to RMS and/or VAX-11 DBMS databases are provided by VAX-11 Datatrieve. A Common Data Dictionary (CDD) is a prerequisite for other than RMS data management. Forms Management is provided by FMS-11, which will be developed further as part of the Common Application Terminal Support (CATS) product set and integrated with the CDD. A Relational Database Management product is under development and should be available prior to VENUS FRS.

In the area of programmer productivity tools, a Transaction Processing product will be available prior to VENUS FRS, and there are several other development and project management utilities being proposed.

GENERAL UTILITIES: Most emphasis here will be on programmer productivity and ease of use. Forms management will be greatly enhanced and its performance improved by merging FMS into the common application terminal subsystem program (CATS/TSS). A second phase, the terminal management subsystem (TMS) will provide a higher level of terminal transparency and performance through the use of 11/23 video terminal concentrators. Transaction processing is also expected to be greatly enhanced by CATS and additional layered software. The VAX Cluster environment, in which VENUS can be used, is a whole set of layered products.

APPLICATIONS: Individual Product Lines will continue to offer applications and tools specific to their marketing efforts, particularly ESG, ECS and PBI, but it is expected that most application software will be provided by joint marketing arrangements with third parties.

6.4 TECHNOLOGY

VENUS is taking advantage of technological innovation in a number of areas: LSI logic, multilayer controlled-impedance backplanes and circuit boards, modular power supplies, mechanical packaging and environmental sensing. Following is a discussion of the functionality of some of these innovations.

Macrocell Arrays

Until now the semiconductor industry has used three approaches to meet the demand for LSI digital circuits: standard off-the-shelf circuit families, custom circuits, and gate arrays. Standard circuits are very economical, but are not sufficient for the complex, specialized functions that VENUS requires. Custom circuits, on the other hand, are quite expensive and regularly have a turnaround time of a year or two. Gate arrays have a shorter turnaround time since the basic array can be fabricated up to metalization, but the interconnecting metal makes the chip larger and increases propagation delays. To provide greater flexibility in circuit design and development, Motorola has created the macrocell approach to custom LSI. This appoach circumvents the cost and time factor of custom circuits and reduces the deficiencies of conventional gate arrays.

The macrocell array is actually an extension of the gate array concept. Instead of gates, however, each cell in the array contains a number of unconnected transistors and resistors. Stored in a computer are the specifications for creating interconnecting patterns that can transform the unconnected transistors and resistors within each cell into SSI/MSI logic functions or "macros". These macros take the form of standard logic elements such as dual type D flip-flops, dual full adders, quad latches, and many other predefined functions. All of these are ECL structures for optimized performance.

The cell library contains 85 macros: 54 for major cells, 14 for interface cells, and 17 for output cells. A single array can contain 106 cells: 48 major, 32 interface, and 26 output. If full adders and

latches are used in all the cells this means a single MCA may contain up to 1192 equivalent gates; if flip-flops and latches are used in all the cells there may be up to 904. Typical power dissipation is 4 watts, 4.4 mW per equivalent gate. Contributing to the high performance of the system as a whole is the extremely low propagation delay in major and interface cells: 1.2-1.8 ns maximum, compared to 3.5-6 for the 10K ECL used in the KL10. Also of considerable importance is the high density: 100 gate equivalents per square inch, compared to 20-30 for MSI. This reduces interconnect delays, thus further enhancing performance, and it also lowers packaging costs as well.

Besides MCAs, technologies considered were the Siemens gate arrays and the Fairchild 100K MSI logic family. The criteria for decision were naturally cost, performance, time to market, multiple sources, and the expected future of the technology. All three technologies meet the performance requirement (4 times 11/780), but in all other categories the decision is between MCA and 100K. The 100K will be available slightly earlier but at 20% greater cost; moreover MSI is definitely not a technology of the future. One problem is second source, but the contract negotiated with Motorola gives Digital the technology/process transfer and license to enable internal second sourcing. Hudson's ability to build MCAs under the transferred process has already been demonstrated.

Circuits

A goal of circuit design is the elimination of all wires on boards and backplanes. This will be accomplished by using 16-layer backplanes and 8-layer pc boards (four signal layers). A further refinement is much greater restriction on the variation in impedance per unit length of etch. We will also increase the number of signal pins available on the edge connectors by adding supplementary connectors to the board solely for power distribution.

Power System

The VENUS power system is configured from various elements of the modular power system (MPS) presently under development by the Power Supply Engineering Group. The MPS consists of an ac-to-dc input module from which several dc-to-dc output modules are powered. The input module rectifies the ac line voltage into a raw 300 Vdc bus. Each output regulator uses constant frequency pulse-width modulation at 50

kHz to convert the 300 Vdc to the desired output voltage. The input module being developed is a 2800-watt three phase. Regulators being developed are 5 volts at 200 and 85 amperes and 2 volts at 100 amperes. Outputs can be paralleled allowing tailoring to specific requirements without excessive unused capacity. Besides attaining efficiencies greater than 70%, use of a 50 kHz switching frequency results in even smaller magnetic components than those obtained at the "standard" 20 kHz switching frequency.

The units can maintain proper operation for up to 5.0 ms of power loss and down to 156 Vac rms line-to-line input voltage. They are mounted side by side above the VENUS logic to be cooled by air exiting from the logic; the configuration is one input module at each end, with seven output regulators between them. Powerup and powerdown sequencing is handled by the EMM. The system provides extensive interface signals for remote diagnosis; e.g. each regulator can be turned on and off by a diagnostic instruction, and monitoring of a module ok signal determines whether the unit is within operating range. The system also has a standby mode in which only the memory array and refresh logic are on, so memory can be preserved while other parts of the machine are being serviced.

Mounted among the regulators in the power supply rack is an EMM board that consists of a pc board and panel, and contains the electronics, fuses and indicators (mostly leds) for both the power system and the environmental sensors. Dc logic voltages will be monitored either by analog comparators or A-D converters; in either case the information is supplied to the console for appropriate action.

A 48-volt battery with built-in charger will back up the memory storage array boards for 10 minutes. The battery output is converted to 300 Vdc and all other regulators are disabled except the +5V unit used for main memory. Also available is battery backup for 100 hours for the time-of-year clock, which is normally powered from an auxiliary +12V output of the input module. In a long power outage, the user may prefer not to run the battery all the way down, as the recharge time is considerable and there may then be no backup for a subsequent minor outage. Thus the system includes a feature that allows the user to disable memory backup.

Recharge Time vs. Usage Time

Battery Time		Recharge
Memory	TOY Clock	Time
10 minutes	100 hours	14-16 hours
10 minutes	10 minutes	4 hours
5 minutes	5 minutes	2 hours
1 minute	1 minute	20 minutes

Mechanical Packaging

New packaging techniques appear at every level of the system, from the cabinet down to the mounting of components on the boards. A large part of the effort expended in dealing with mechanical and environmental issues is in setting standards and then getting vendors to provide equipment that meets those standards, but various innovations have also been developed by Digital's own engineers.

It is expected that almost all VENUS systems will be installed in computer rooms with a raised floor, under which pass not only the cables and other utilities, but also conditioned air. The overall packaging scheme takes advantage of this physical environment by ducting the bottom of the cabinet into this source of cooling air, which passes under pressure up through the card cage. (At installations without a raised floor, air will be drawn in through louvers at the bottom front of the cabinet.) Air then flows by the power supplies, and the blower on top of the cabinet expels it at the rear through mufflers that keep the noise level well within the acoustic limit of 60 dbA. The 10K ECL and other standard circuit components are cooled directly by the air flowing between the boards. MCAs however dissipate too much heat to be cooled in this manner. Hence mounted on the MCAs are special sinks that dissipate heat into the passing air with much greater efficiency.

Modules are the new L type that are the same height as hex boards but have three sets of pin connectors. These connectors are not only denser than the connectors on the old boards, but they also protrude through the backplane so cable connectors can be mounted directly on them, eliminating the space wasted by having slots just for connectors. Between the sets of pins are pads that connect to an aluminum ground frame that is an integral part of the card cage (the entire frame thus serves as logic ground). Copper bars at the top and bottom of the backplanes carry dc voltages that are picked up by pads at the top and bottom of the cards. Although cables still connect the

power supplies to the card area, use of these voltage and ground bars combined with placing the power supplies above the card cage eliminates a great deal of the power cabling that made the inside of older machines look so cluttered. Some of the module pins must still be used for power and grounds, but the new arrangement leaves 230 pins available for signals on each module compared to about 168 on the old hex boards.

Another packaging innovation is the use of sockets for RAMs and MCAs. Sockets increase base system cost, but they will decrease maintenance cost, yielding a net, discounted life cycle cost saving, because of the convenience with which individual chips can be removed and replaced.

Environmental Monitoring

Located throughout the cabinet are devices for sensing various environmental conditions. The electronics and indicators associated with these devices are on the monitor board mounted in the power supply rack. In most cases, conditions are reported to the console for appropriate action.

The principal environmental concern is overheating in the logic, as the junction temperature in the MCAs directly affects their failure rate, which doubles with every rise of 20 degrees C. At a junction temperature of 88 degrees C, the failure rate is 360 per billion hours. Measurements show that incoming air with an ambient temperature of about 24 degrees C produces junction temperatures in the range of 100 to 107 degrees C. To guard against overheating, precise thermistors are used to monitor the ambient temperature of the incoming air and the temperature gradient across the card cage. When the inlet air temperature below the card cage is sensed to be 32 degrees C, the monitor module issues a warning to the system console. When the inlet temperature reaches 42 degrees C, the monitor module shuts off system power. By comparing the temperature of the inlet air with that of the air above the card cage, the monitor module can determine the temperature rise incurred by cooling the system logic. When that rise exceeds 20 degrees C, system power is shut off.

Another important feature of the monitor module is measuring the output voltages of the power supply. If any one is found to violate a predetermined limit, the monitor module reports the violation to the system console. Power supply voltages must be of the correct values to insure solid system operation. The voltages

are continually measured so that discrepant readings can be reported and corrective maintenance solicited.

Other environmental features include devices for detecting an overheated regulator or failed blower. Overheating of a regulator, whether caused by faulty operation or too high an ambient temperature, closes a thermal switch that shuts down the main power control. Unless accompanied by a temperature problem, failure of a blower is not serious enough to warrant automatic corrective action, but it is still desirable to report such an event.

APPENDIX A - VENUS REQUIREMENTS

VENUS REQUIREMENTS - PROTOTYPE 1 MAIN USER - CPU DEVELOPMENT

	PROTOTYPE 1	QUANTITY ORDERED	DATE REQUIRED
MEMORY ARRAY	4 MB (4 MB ARRAY)	1	3/1/83
	8 MB (1 MR ARRAY)	8	9/1/83
SBIA		2	8/1/83
SBI BUS	DR780	1	7/15/82
SBI BUS	DW780-MA	2	7/15/82
	C1780-MA	1	7/15/82
	RH780-AA	1	2/15/83
	H9602 SBI EXP. CAB.	1	2/15/83
UNIBUS EQUIP.	DMF32-AC	2	7/15/82
	VT200	8	7/15/82
	LP07-GA	1	7/15/82
	VT100-AA	1	7/15/82
	H9602 } UNIBUS	1	7/15/82
	DD11-CK } EXP.	1	7/15/82
	BA11-AE } CAB.	1	7/15/82
	DD11-DK }	3	7/15/82
	DEUNA-AA	1	2/15/83
	RX211-BA	1	7/15/82
	RK711-EA	1	7/15/82
	LA120-DA	1	7/15/82
	H4000	1	2/15/83
	PLUTO (DECSA-AA)	1	8/15/83
	M3103 (LP/CR)	1	8/15/83
	M3102 (ASYNC)	1	8/15/83
	DMH32	1	8/15/83
	BNE3A-10	1	8/15/83
	BNE2A-MA	1	8/15/83
FRONT END CAB.	RLV12	1	5/15/82
	RL02-AK	1	5/15/82
CI EQUIP.	HSC50	1	10/15/82
	RA81-CA (WITH CAB.)	1	10/15/82
	TA78-BB	1	10/15/82
	SC008-AA	1	10/15/82
	BNCIA-10	2	10/15/82
	K.SDI	1	10/15/82
	K.STI	1	10/15/82

VENUS REQUIREMENTS - PROTOTYPE 1 (CONT.)

PROTOTYPE 1		QUANTITY ORDERED	DATE REQUIRED
IDTC EQUIP.	UDA52	1	7/15/82
	RA60-CA	1	7/15/82
	TU81	1	7/15/82
MASSBUS EQUIP.	RP06-BA	1	2/15/83
	TU77-FB	1	2/15/83
EXTENDERS	L0300 (L-ECL)	4	7/26/82
	L0300-YA (L-TTL)	2	7/26/82
	L9102 (L-CI780)	1	7/26/82
	L9102-YA (L-CI780)	1	7/26/82
	W904 (STD. HEX)	1	7/26/82
	W984 (DOUBLE WIDTH HEX)	1	7/26/82
	W9025 (EXTENDED HEX)	1	7/26/82
CABLES	BC06Z-25 (MASSBUS)	1	7/26/82
	BC03M-25 (MODEM CABLE)	5	7/26/82
	BC05L-15	6	7/26/82
	70-14246-15 (UNIBUS)	2	7/26/82
	BC11A-15 (UNIBUS)	2	7/26/82
	BC05L-08	4	7/26/82
	17-00087-08 (SBI)	6	7/26/82
TERMINATORS	70-9938 (MASSBUS)	1	7/26/82
	M9302 (UNIBUS)	1	7/26/82
	M9400-YE (QBUS)	1	7/26/82
HEADERS	M9014 (UNIBUS)	2	7/26/82
	M9401 (QBUS)	2	7/26/82

VENUS REQUIREMENTS - PROTOTYPE 2: MAIN USER - CPU DEVELOPMENT

PROTOTYPE 2		QUANTITY ORDERED	DATE REQUIRED
MEMORY ARRAY	4 MB (4 MB ARRAY)	1	7/1/83
	2 MB (1 MB ARRAY)	2	9/1/82
SBIA		2	9/1/82
SBI BUS ADAPTERS	DW780-MA	2	7/15/82
	CI780-MA	1	7/15/82
	RH780-AA	1	2/15/83
	RH780	1	2/15/83
	H9602	1	2/15/83
	SBI EXP. CAB.		
UNIBUS EQUIP.	DMF32-AC	2	7/15/82
	VT200	8	7/15/82
	LP07-GA	1	7/15/82
	H9602 } Unibus	1	7/15/82
	BA11-KE } Exp.	1	7/15/82
	DD11-DK } Cab.	3	7/15/82
	H4000	1	2/15/83
	DEUNA-AA	1	2/15/83
	BNE3A-10	1	2/15/83
	BNE2A-MA	1	2/15/83
	RK711-EA	1	7/15/82
	RX211-BA	1	7/15/82
	LA120-DA	1	7/15/82
	VS100 (GEMSTONE)	1	8/1/83
	DMH32	1	6/1/83
FRONT END CAB.	RLV12	1	5/1/82
	RL02-AK	1	5/1/82
CI EQUIP.	HSC50	1	2/15/83
	RA81-AA	2	2/15/83
	RA81-CA	1	2/15/83
	TA78-BB	1	2/15/83
	SC008-AA	1	2/15/83
	BNCIA-10	2	2/15/83
	K.STI	1	2/15/83
	K.SDI	1	2/15/83
IDTC EQUIP.	UDA52	1	12/15/82
	RA60-CA	1	12/15/82
	TU81	1	12/15/82

VENUS REQUIREMENTS - PROTOTYPE 2 (CONT.)

PROTOTYPE 2		QUANTITY ORDERED	DATE REQUIRED
EXTENDERS	L0300 (L-ECL)	4	7/15/82
	L0300-YA (L-TTL)	2	7/15/82
	L9102 (L-CI780)	1	7/15/82
	L9102-YA (L-CI780)	1	7/15/82
	W904 (STD. HEX)	1	7/15/82
	W984 (DOUBLE WIDTH HEX)	1	7/15/82
	W9025 (EXTENDED HEX)	1	7/15/82
CABLES	BC06Z-25 (MASSBUS)	1	7/15/82
	BC03M-25 (MODEM)	5	7/15/82
	17-00087-08 (SBI)	6	7/15/82
	70-14246-15 (UNIBUS)	2	7/15/82
	BC11A-15 (UNIBUS)	3	7/15/82
	BC05L-08	5	7/15/82
TERMINATORS	70-9938 (MASSBUS)	1	7/15/82
	M9302 (UNIBUS)	1	7/15/82
HEADERS	M9014 (UNIBUS)	1	7/15/82

VENUS REQUIREMENTS - PROTOTYPE 3 MAIN USER - VMS DEVELOPMENT

	PROTOTYPE 3	QUANTITY ORDERED
DATE REQUIRED:	2/1/83	
MEMORY ARRAY	24 MB (4 MB ARRAY)	6 (8/1/83)
	4 MB (1 MB ARRAY)	4
SBIA		2
SBI BUS	DR780	1
	DW780-MA	2
	C1780-MA	1
	RH780-AA	1
	RH780	1
	H9602	1
	SBI EXP. CAB.	
UNIBUS EQUIP.	DMF32-AC	2
	VT200	8
	LP07-GA	1
	VT100-AA	1
	DD11-CK } EXP.	1
	BA11-AL } CAB.	1
	DD11-DK	3
	DEUNA-AA	1
	RX211-BA	1
	RK711-EA	1
	LA120-DA	1
	H4000	1
	BNE3A-10	1
	BNE2A-MA	1
	H9602	1
FRONT END CAB.	RLV12	1
	RL02-AK	1
CI EQUIP.	HSC50	1
	RA81-CA	1
	TA78-BB	1
	SC008-AA	1
	BNCIA-10	2
	K.SDI	1
	K.STI	1
IDTC EQUIP.	UDA52	1
	RA60-CA	1
	TU81	1
MASSBUS EQUIP.	RP06-BA	1
	TU77-FB	1

VENUS REQUIREMENTS - PROTOTYPE 3 (CONT.)

		QUANTITY ORDERED
DATE REQUIRED:	2/1/83	
EXTENDERS	L0300 (L-ECL)	2
	L0300-YA (L-TTL)	2
CABLES	BC06Z-25 (MASSBUS)	1
	BC03M-25 (MODEM)	2
	70-14246-15 (UNIBUS)	1
TERMINATORS	70-9938 (MASSBUS)	1
	M9302 (UNIBUS)	1
HEADERS	M9014 (UNIBUS)	1

VENUS REQUIREMENTS - PROTOTYPE 4 MAIN USER - SYSTEM QUALIFICATION
(DVT, SPT, PRELIM. QUAL.)

	PROTOTYPE 4	QUANTITY ORDERED	
DATE REQUIRED:	1/1/83		
MEMORY ARRAY	1 MB (1 MB ARRAY)	1	
	32 MB (4 MB ARRAY)	8	(9/1/83)
SBIA		2	
SBI BUS ADAPTERS	DW780-MA	3	
	C1780-MA	2	
	DR780	2	
	RH780-AA	2	
	H9602 SBI.EXP.CAB.	1	
UNIBUS EQUIP.	DMF32-AC	16	
	VT100-AA	2	
	LP26-EB	1	
	H9602 } UNIBUS	2	
	BA11-AL } EXP.	4	
	DD11-DK } CAB.	12	
	LA34-DA	1	
	LA120-DA	1	
	VT200	1	
	LP25-AA	1	
	LN01	1	
	DMR11-AA	1	
	DMP11-AA	1	
	DUP11-DA	1	
	DZ11-C	1	
	DZ11-D	1	
	DZ11-F	1	
	DEUNA-AA	1	
	DR11-W	2	
	H4000	1	
	PLUTO (DECSA-AA)	1	
	M3103 (LP/CR)	1	
	M3102 (ASYNC)	1	
	BNE2A-MC (300 NI CABLE)	1	
	BNE3A-20 (20M CABLE)	1	
	VS100	4	
	DMH32	4	
FRONT END CAB.	RLV12	1	
	RL02-AK	1	

VENUS REQUIREMENTS - PROTOTYPE 4 (CONT.)

PROTOTYPE 4		QUANTITY ORDERED
CI EQUIP.	HSC50	1
	RA81-CA	2
	RA81-AA	1
	TA78-BB	1
	SC008-AA	1
	BNCIA-10	4
	K.SDI	5
	K.STI	1
IDTC EQUIP.	UDA52	1
	RA60-CA	2
	TU81-CA	1
MASSBUS EQUIP.	RM05-BA	1
	RP07-BA	4
	TU78-AB	1
	TU78-AF	1
EXTENDERS	L0300 (L-ECL)	2
	L0300-YA (L-TTL)	2
CABLES	BC06Z-25 (MASSBUS)	1
	BC03M-25 (MODEM)	2
	70-14246-15 (UNIBUS)	2
TERMINATOR	70-9938 (MASSBUS)	1
	M9302 (UNIBUS)	2
HEADERS	M9014 (UNIBUS)	2

VENUS REQUIREMENTS - PROTOTYPE 5 MAIN USER - IO ENGINEERING & DIAGNOSTICS

PROTOTYPE 5		QUANTITY ORDERED
DATE REQUIRED:	4/1/83	
MEMORY ARRAY	4 MB (4 MB ARRAY)	1 (1/2/84)
	4 MB (1 MB ARRAY)	4
SBIA		2
SBI BUS	DW780-MA	3
	C1780-MA	2
	DR780	2
	DR780-AA	2
	RH780	2
	RH780-AA	2
	H9602	2
	SBI EXP. CAB.	
UNIBUS EQUIP.	DMF32-AC	2
	DB11-A	1
	VT100-AA	1
	LP26-EB	1
	DMP11-AA	1
	DMP11-AB	1
	DMP11-AC	1
	DMP11-AE	1
	DMR11-AA	1
	DMR11-AC	1
	VT200	1
	DZ32-C	1
	H9602 } UNIBUS	2
	BA11-AL } EXP.	1
	DD11-DK } CAB.	3
	LP07-GA	1
	LA34-DA	1
	LP25-BA	1
	LA120-DA	1
	RX211-BA	1
	DEUNA-AA	1
	DUP11-DA	1
	RK711-EA	1
	DR11-W	1
	H312-A	1
	DC05D CABLE	1
	LA38-HA	1
	LP11-CA	1
	TS11-BA	1
	LPA11-K	1

VENUS REQUIREMENTS - PROTOTYPE 5 (CONT.)

	PROTOTYPE 5	QUANTITY ORDERED	
UNIBUS EQUIP. (CONT.)			
	BNE3A-10	1	
	BNE2A-MA	1	
	H4000	1	
	DECSA-AA (PLUTO)	1	
	M3103 (LP/CR)	1	
	M3102 (ASYNC)	1	
	VS100 (GEMSTONE)	1	
	DMH32	2	
FRONT END CAB.	RLV12	1	
	RL02-AK	1	
CI EQUIP.	HSC50	1	
	RA81-AA	1	
	RA81-CA	1	
	TA78-BB	1	
	SC008-AA	1	
	BNCIA-10	3	
	RA80-BA	1	
	K.STI	1	
	K.SDI	1	
IDTC EQUIP.	UDA52	1	
	RA60-CA	1	
	TU81	1	
MASSBUS EQUIP.	RP06-BA	1	
	RM80-BA	1	
	RM05-BA	1	
	RM03-BA	1	
	RP07-BA	1	
	TU77-FB	1	
	TU78-AF	1	
	TU45-KA	1	
	TEE16-AE	1	(CANCEL-PHASE OUT FY84)

VENUS REQUIREMENTS - PROTOTYPE 5 (CONT.)

PROTOTYPE 5		QUANTITY ORDERED
EXTENDERS	L0300 (L-ECL)	2
	L0300-YA (L-TTL)	2
	L9102 (L-CI780)	1
	L9102-YA (L-CI780)	1
	W904 (STD. HEX)	1
	W984 (DOUBLE WIDTH HEX)	1
	W9025 (EXTENDED HEX)	1
CABLES	BC06Z-25 (MASSBUS)	1
	BC03M-25 (MODEM)	5
	70-14246-15 (UNIBUS)	2
TERMINATOR	70-9938 (MASSBUS)	1
	M9302 (UNIBUS)	2
HEADER	M9014 (UNIBUS)	2

VENUS REQUIREMENTS - PROTOTYPE 6 MAIN USER - PRELIM. 102 & FCC TESTING

	PROTOTYPE 6	QUANTITY ORDERED
DATE REQUIRED:	3/15/83	
MEMORY ARRAY	4 (4 MB ARRAY)	1 (9/3/83)
	8 (1 MB ARRAY)	8
SBIA		2
SBI BUS ADAPTERS	DW780-MA	3
	C1780-MA	1
	DR780-AA	1
	RH780-AA	1
	H9602	1
	SBI EXP. CAB.	
UNIBUS EQUIP.	DMF32-AC	2
	VT100-AA	1
	VT200	1
	DEUNA-AA	1
	DECSA-AA (PLUTO)	1
	M3102 (DECSA-LC)	1
	M3103 (DECSA-LD)	1
	BNE3A-10	1
	BNE2A-MA	1
	DR11-W	1
	H9602 } UNIBUS	1
	BA11-AL } EXP.	1
	DD11-DK } CAB.	3
	LA120-DA	1
	LP06-YA	1
	LPA11-K	1
	H312-A	1
	BC050D Cable	1
	H4000	1
FRONT END CAB.	RLV12	1
	RL02-AK	1
CI EQUIP.	HSC50	1
	RA81	1
	TA78-BA	1
	SC008	1
	BNCIA-10	2
	K.SDI	1
	K.STI	1

VENUS REQUIREMENTS - PROTOTYPE 6 (CONT.)

PROTOTYPE 6		QUANTITY ORDERED
IDTC EQUIP.	UDA52	1
	RA60	1
	TU81	1
MASSBUS EQUIP.	TEE16-AE	1
	RP06-BA	1
EXTENDERS	L0300 (L-ECL)	2
	L0300-YA (L-TTL)	1

VENUS REQUIREMENTS - SYSTEM #49 MAIN USER - FINAL 102 TESTING

SYSTEM #49		QUANTITY ORDERED
DATE REQUIRED:	8/83	
MEMORY ARRAY	1 (MB ARRAY)	1
SBIA		1
SBI BUS ADAPTERS	DW780-MA	2
UNIBUS EQUIP.	DMF32-AC	1
	VT100-AA	2
	LA120-DA	1
FRONT END CAB.	RLV12	1
	RL02-AK	1
IDTC EQUIP.	UDA52	1
	RA60-CA	1
	TU81-CA	1
EXTENDERS	L0300 (L-ECL)	2
	L0300-YA (L-TTL)	1
CABLES	BC06Z-25 (MASSBUS)	1
	BC03M-25 (MODEM)	2
	70-14246-15 (UNIBUS)	1
	BC11A-15 (UNIBUS)	1
TERMINATOR	70-9938 (MASSBUS)	1
	M9302 (UNIBUS)	2
HEADER	M9014 (UNIBUS)	2

APPENDIX B - PRODUCT REQUIREMENTS: ENGINEERING RESPONSE

Summarized below are the requirements set forth in the VENUS Product Requirements Document by Carl Gibson. With each item is Engineering's response. In this list the following abbreviations are used:

B Basic system (CI Base)
T Typical system
M Maximum system

General

Customer satisfaction superior to comparable IBM
On the presumption that this is primarily a RAMP issue, we are working to achieve this goal. We believe there is nothing in the hardware that would prevent our achieving it.

CPU with CIS and warm floating point (G & H) -- yes.

Console with terminal and load device -- yes.

Vector processor available
We will make sure the FPS AP120B or equivalent is available. There is no plan for a DEC-designed vector processor.

FPA available -- yes.

User accessible control store with software tools
Writable control store for all microcode, accessible through console only (i.e. system halted). There will be VENUS macros for tools similar to those presently available for 11/780.

B: single cabinet with expansion space
Disk and tape drives, line printer, console and other terminals are not included in basic double-width cabinet. Every system requires a separate Unibus cabinet. Stepdown transformer required outside North America is not in basic cabinet. Otherwise, yes.

Single cabinet capacity
CPU with FPA -- yes.
8 MB memory -- yes.
32 async lines -- in Unibus cabinet.
6-8 sync lines -- in Unibus cabinet.
1 line printer -- control in Unibus cabinet.
1 card reader -- control in Unibus cabinet.
600 MB disk -- no.
Magnetic tape subsystem -- no.

Dock mergeable -- yes except for CR11 and special equipment.

DR32 on A bus
We recommend using the DR780 on the SBI. The requirement of providing up to 4 real time interfaces can best be satisfied in this manner. One A bus tap is provided for CSS or the Product Lines to design DR-type or other foreign devices.

Performance

Overall $\geq$ 4 x 11/780 -- yes, will make 4.

> 3 mips -- yes.

FPA > 4 x 11/780 FPA -- yes, will make 4.

Interactive performance < 3 seconds
(excluding application computation)
Taking a workload for which the 11/780 with Massbus disks has a response time of 3 seconds, VENUS will run 3 times as many copies of the workload at 3 seconds provided it has HSC disks and 3 times the memory.

33 decimal figures accuracy
Accuracy is a matter of correctness. We will provide 33 digits of precision in H floating; results accurate within that precision.

Context switching < 50 us -- not feasible.
The memory references required in LDPCTX and SVPCTX alone account for about 40 us, and clearing the translation buffer takes about 10 us more. Software overhead appears on top of that. Jud's best estimate is under 200 us per context switch, as measured by two processes setting each other's local event flags.

Scicomp $\geq$ 3.5 x 11/780 -- yes, looks good (with FPA).

ECS workload @ 3 x 11/780 -- yes.
3 times the work in the same time, with HSC50 disk controller.

Realtime
Handle 3 x as many 16-bit data samples as faster of Comet and 11/780
Yes - up to the limit imposed by the buses (Unibus for DR11 or LPA11, SBI for DR780); note that unlike 11/780, VENUS can have separate SBI and Unibus for the device.
Handle 4 devices @ 2-4 MB/second -- yes.
With smaller VAXes as front ends, provide 3 x as many links as 11/780, or 3.5 x as many cycles for background scicomp -- yes.

Context switching, call and interrupt response/service ≥ 3 x the faster of Comet and 11/780 -- yes.

IO handling 16 MB/second -- yes.

Handle simultaneously 4 sync lines @ 100 kbps for graphics with minimum CPU degradation -- yes, with ESG 11C03 "Fastek" option on unibus.

Handle simultaneously 4 public parallel DMA ports @ 4 MB/second -- yes.

Unibus bandwidth ≥ 11/45 -- no, same as 11/780.

350% of 11/780 throughput -- workload dependent.

Timeshare 512 terminals simultaneously -- no.
VMS can support 128 users adequately now, so VENUS should be able to support at least 256 users doing the same type of job. Note that the physical number of terminals is not VMS limited.

Handle IO load equivalent to 4 Unibuses, 8 Massbuses and maximum intersystem connections -- yes.

Owner tune system to within 90% of theoretical maximum throughput for application code (acquire skill for this in 16 hours) -- no.
We wouldn't know how to predict theoretical maximum throughput, and we doubt that an arbitrarily selected owner could learn how to tune in 16 hours. VMS is constantly reducing the amount of technical expertise needed for optimal tuning of the system.

Transaction processing
10-500 terminals on line simultaneously in network -- yes.
3 x as many application terminals as 11/780 -- yes.
Concurrent with program development -- yes.

FORTRAN and COBOL performance = IBM 3031 (370/158) with optional performance = 3032(370/168)
There are no performance options for COBOL. With an FPA, both FORTRAN and COBOL will outperform a 370/168.

Cost

Transfer cost
B: 40K -- no; best estimate is 73K.
T: < 70K -- no.

Cost of ownership < 11/780 -- yes.

FPA = 11/780 FPA -- no; estimate 3.5K.

BMC $\leq$ 1.5% of transfer cost -- TBD in Phase 3.

RAMP

Remote diagnostics -- yes.

Console port with online diagnostics -- yes.

UETP -- yes.

MTBF much greater than 11/780 -- yes.

No more than 1 crash per month
"Crash" means the system is down for all users. Restrictions are that the system is: all DEC equipment unmodified, under DEC contract, up to ECO level, operated within power and environmental specs, without user privileged code. With these restrictions, the software meets the requirement; the hardware MTBF for the CI base is 420 hours, but the requirement can be met by installing redundant peripheral support.

No more than 1 unscheduled outage for repairs per 3 month period
Achievable on DMT configuration; not on the system unless repair of peripherals is not "outage".

Interconnects

SBI for Unibus peripherals on DW780
B: optional -- standard
M: 4 -- only 2

CI on M -- yes

Interconnects to IBM (bisync), CDC, Univac, Honeywell
IBM yes; others if software developed.

VAX Cluster configurations -- yes.

Capable of handling at least 2 intersystem buses -- yes.

36-bit to DECsystem-20 -- CI DECnet between VAX/VMS and TOPS-20 is not committed at this time. Disk sharing between 32-bit and 36-bit systems will not be supported by the CI architecture.

Availability

FRS - Q4/FY82 -- 6/84.

Volume - Q2/FY83 -- see Figure 3.2.

FRS: All languages and software tools -- see Software Section.

All hardware except:

FRS + 3 months: 40-80 MB removable disk -- no.

FRS + 6 months: Vector processor -- no.
DR32 on A bus -- no.

FRS + 9 months: Maximum memory -- at FRS.
Maximum system -- at FRS.
Tapes -- at FRS.

FRS + 12 months: 4 CI -- yes.
SBI with 2 UBAs & 4 MBAs -- yes.

IO Equipment

Disk (fixed or fixed/removable with optional dual channel access)
B: 600 MB -- 456 MB.
T: 1 GB -- yes.
M: 20 GB -- yes.

Tape
B: 1600/6250 bpi, 125 ips -- yes.
T: 2 6250 bpi, 200 ips -- 125 ips.
M: 8 top line -- 6250 bpi, 125 ips.

Async lines
B: 16 @ 1200 b -- yes.
T: 32 @ 2400 b -- yes.
M: 256 @ 2400 b -- yes.

Sync lines
T: 2 @ 100 kb or 8 @ 9600 b (64 terminals) -- yes.
M: 4 @ 100 kb or 16 @ 9600 b (512 terminals) -- yes.

Line printer (M: 4) -- yes.

Card reader (M: 2) -- yes.

Intelligent communication subsystem (Mercury) -- yes (NI/Pluto).

Terminal cluster controller -- TDMS/D dependent.

Intelligent terminals with downline load -- TDMS/D dependent.

Terminal types
Multidrop -- TDMS/D dependent.
VT100 style -- yes.
PDT style -- no.
GIGI -- yes.

Typeset -- PBI Product Line dependent.

MA780 -- no.

DR780 -- yes.

Software

VAX/VMS -- yes.

Languages

All layered products are available separately.

FORTRAN IV-PLUS -- yes (VAX-11 FORTRAN).
Interactive and commercial BASIC -- yes (VAX-11 BASIC).
BASIC-PLUS-2 -- replaced by VAX-11 BASIC.
PASCAL -- yes.
ADA -- under development.
CORAL-66 -- yes.
PEARL -- no.
COBOL -- yes.
MUMPS -- yes (now called VAX-11 DSM).
BLISS -- yes.
PL/I -- yes.
APL -- under development.
SORT/MERGE -- bundled with VAX/VMS.
ALGOL -- no.
LISP -- under consideration.
RPG-II -- under development.
TRAX-32 -- under development (now called ACMS).
(Not considered a traditional language.)

Syntax checkers and symbolic debuggers for all languages
Symbolic debuggers in all languages, syntax checkers (i.e. check without compile) in many.

Language support for vector processor -- no.

Data management
In VMS (RMS), plus VAX-11 DBMS (CODASYL compliant). Relational DBMS under development.

Form language compiler -- yes.

Message control with transaction roll forward/backward, journalling, shadow recording -- yes.

Multivolume disk files -- yes.

ANSI standard tape handling -- yes.

IBM tape handling
Support industry standard tape format - there are

currently no plans to support IBM tape subsystems.

Multiple operator consoles -- yes.

Unattended batch -- yes.

DECnet, X25, IBM (SNA) -- yes.

Distributed data base management (DBMS-32)
Yes, through Datatrieve.

Routines for graphic displays and plotters
These are Product Line specific.

Global optimizer -- probably for FORTRAN.V4.

File exchange utilities for other DEC -- yes.

Application packages: statistics, project management/control, math library, CAI, school administration
Math in runtime library; some CAI, but otherwise these items must be funded by Product Lines; project management/control through VAX-11 CMS and TCS.

Fully supported end-user tools for UCS or equivalent -- no.
(See remarks under General category.)

System- & network-wide data directory & dictionary -- yes.

Tools for network performance measurement, load balancing, tuning reconfiguring -- yes. (not automatic)

Automatic VMS tuning invokable by user (must achieve > 75% of maximum theoretical throughput on average) -- no.
VMS automatically adjusts the working set and the swap rate according to limits set by the system manager. Future releases are expected to do more in this direction, but the ultimate goal is to make tuning unnecessary on normal workloads.

Word processing -- yes.

Tools for computer-assisted program documentation -- yes, planned.

Typesetting -- yes.

Inquiry language, report writer (VAX-11 Datatrieve) -- yes.

Job class scheduling -- not useful in VMS.

System resource accounting -- yes.

Disk allocation control & reporting -- yes.

Removable private files -- yes.

System library manager -- yes.

System security & protection -- yes.

Dynamic working set size selection -- yes.

Sharable programs -- yes.

Routines for RSTS migration -- VAX-11 BASIC.
Also specific documentation.

Cross-system development for RSX-11M, RSX-11S, RT-11, RT2
RSX yes, RT yes.

VAX Cluster support -- yes.

Support of all devices on 11/780, Comet, Nebula, VAX Cluster, Fonz, SCS, PDT
Yes for 11/780, Comet, Nebula, VAX Cluster; others must be determined on a case-by-case basis.

APPENDIX C - WHO'S WHO IN THE VENUS PROGRAM

Product Management

Carl Gibson	MRO1-2/E47	231-6779	LVE System Product Mgr
Ruth Jobin	MRO1-2/E47	231-6732	Administrative Secretary
Peter Ross	MRO1-2/E47	231-4471	LVE SW Product Mgr
Peter Schay	MRO1-2/E47	231-5784	LVE HW Product Mgr
Barbara Watterson	MRO1-2/G6	231-7527	Process Analyst

Marketing Team

Eli Anfenger	PKO3-1/M28	223-2210	TVG
Joe Austin	MLO3-6/E94	223-8897	Memory Group
Al Avery	TWO/C04	247-2115	Current VAX Sys Group
Alan Belancik	MKO1-1/E25	264-5033	TIG
Ron Brown	CXO	522-2251	Mass Storage Group
Prem Chawla	PKO3-1/M56	223-5456	TOEM
Dave Chen	MKO1/1-D29	264-4435	TIG
Bill Clark	MRO1-1/M40	231-5617	ECS
Howard Coffman	MKO1-2/C13	264-4961	MDC
Bill Colquitt	MKO1-2/K34	264-8705	CSI
Peter Damon	ZKO1-2/C7	264-8502	CSSE
Bob Flynn	MLO3-6/E94	223-1850	Mass Storage Group
Abbot Gilman	MRO1-1/M75	231-4627	ESG
Donna Graves	MKO1-2/N38	264-5420	Commercial Group
Bill Grimes	MKO1-2/H32	264-7830	COEM
Nikki Hartnett	MRO1-1/M40	231-4333	ECS
Gim Hom	PKO3-1/S93	223-1349	Customer Services Group
Karen Kilday	MRO1-1/A65	231-7496	Tech Products Group
Duane Lashua	CFO2-2/J21	251-1243	IEG
Nicky Lecaroz	MKO1-2/N35	264-8893	CSI
Jeff Levitt	HUO	225-4281	MSG
Dave MacDonald	HDO	264-4710	CSS
Linda Moore	MRO1-1/M42	231-5262	ESG
Hap Prindle	MRO2-3/M84	231-6239	LDP
Guy Marque Pucheu	GE	x2765	European Marketing Group
Tom Rarich	TWO/C11	247-2458	Dist Sys Group
Dick Rislove	MKO1-2/N38	264-5281	Commercial Group
Steve Rothman	VWO	289-6217	32-Bit Program Office
Toni Rudnicki	MKO1-2/A13	264-4318	MDC
Linda Sarles	PKO3-1/M56	223-3293	TOEM
Len Slozek	MKO1-2/H32	264-5475	COEM
Kevin Smith	MLO3-6/E94	223-5880	Mass Storage Group
Phil Spiro	VRO5-2/C10	273-3067	DIS
Tony Sukiennik	MKO1-2/K34	264-6689	CSI
Dave Walker	HZO	264-4539	GSG
Ken Walker	MKO1-2/B11	264-6111	PBI
Joyce Znamierowski	MKO1-2/H32	264-7829	COEM

Large System Group Administration

Gordon Bell	MRO1-2/E78	231-4650	Senior VP of Engrg
Dave Copeland	MRO1-2/E74	231-4012	LSG Site Engrg
Ulf Fagerquist	MRO1-2/E78	231-6408	LSG Senior Group Mgr
Greg Gaines	MRO1-2/E16	231-6300	Personnel Rep
Pat Haslam	MRO1-2/E47	231-6486	Engrg Administrator
Diane Lorion	MRO1-2/E78	231-6282	Product Mgt Administrator
Susannah Nathan	MRO1-2/E16	231-6301	Educational Consultant
Roy Rezac	MRO1-2/E18	231-4140	Logical CAD Mgr
David Sawin	MRO1-2/E78	231-5965	LSG Financial Mgr
Earl Van Horn	MRO1-2/E78	231-6728	ISPS Modelling
Charlie Williams	MRO1-2/E78	231-6196	Financial Analyst

Hardware Engineering

Robert Albertine	MRO1-2/E47	231-4170	Principal Engineer
Al Anderson	MRO1-2/E47	231-4798	Clock Distribution Engr
Ed Anton	MRO1-2/E47	231-6200	Console Design Engr
Scott Arnold	MRO1-2/E47	231-4413	M Box Engrg Tech
Ron Ashey	MRO1-2/E47	231-7130	M Box Tech
Dennis Balboni	MRO1-2/E47	231-4781	E Box Tech
Mohammed Bari	MRO1-2/E47	231-6401	EMI/RFI Engr
Dick Bisson	MRO1-2/E47	231-4779	I Box Tech
Bob Blackledge	CXO/P13	522-2329	HSC50 Hardware Supv
Ginny Blaha	MRO1-2/E47	231-6512	F Box Design Engr
John Bloem	MRO1-2/E47	231-6209	I Box Development Mgr
Bob Boisse	MRO1-2/E47	231-6644	Tech
Wayne Boland	MRO1-2/E47	231-7530	E Box Tech
John Borg	MRO1-2/E47	231-4795	Power Supply Design Engr
Ray Boucher	MRO1-2/E47	231-4422	F Box Design Engr
Ken Brabitz	HLO2-2/N11	225-5059	LSI Program Mgr
Bill Bruckert	MRO1-2/E47	231-6293	M Box Project Ldr
Don Bussolari	MRO1-2/E18	231-6441	Electromechanical Tech
Chuck Butala	MRO1-2/E47	231-4766	Power Supply Supv
Jim Calvo	MRO1-2/E47	231-5923	MCA & PC Scheduler
Pat Cappabianca	MRO1-2/E47	231-4796	Mechanical Engr
Nick Cappello	MRO1-2/E18	231-6261	Engrg Services Mgr
Steven Chenetz	MRO1-2/E47	231-7519	Circuit Engr
Derrick Chin	MRO1-2/E47	231-6719	Circuit Technology Supv
John Cross	MRO1-2/G6	231-7774	Principal Engr
John Crossin	MRO1-2/E47	231-5933	Memory Expansion Project Ldr
Gerry DeGrace	MRO1-2/G5	231-6418	Project Planner
Steve Delahunt	MRO1-2/E47	231-4321	Engr
Corinne DeLegge	MRO1-2/E47	231-5919	Secretary
Al Dellicicchi	MRO1-2/E47	231-6104	M Box Design Engr
John DeRosa	MRO1-2/E47	231-5679	Microprogrammer
Dick Doucette	HLO1-1/R11	225-4920	MCA Circuit Engr
Andy Douglass	MRO1-2/E47	231-7518	Power and Package Design
Bill Doyle	MRO1-2/E47	231-4808	Mechanical Tech
John Drasher	HLO1-1/Q05	225-4936	IDEA Engr
Tom Eggers	MRO1-2/E47	231-4964	E Box Project Ldr
Dave Ellis	MLO21-2/E64	223-6568	Electronic Storage Devel Mgr

Bill English	MRO1-2/E47	231-4785	Documentation Consultant
Mike Evans	MRO1-2/E47	231-7771	Design Engr
John Ewalt	MRO1-2/M53	231-7590	Release & Documentation Mgr
Joe Farrell	MRO1-2/E69	231-5005	Computer Services Ops Analyst
Linda Feldeisen	MRO1-2/E69	231-4539	LSG User Services Supv
Mike Flynn	MRO1-2/E47	231-4413	M Box Engr
Tryggve Fossum	MRO1-2/E47	231-6285	Microcode & F Box Project Ldr
Mike Gallant	MRO1-2/E47	231-6545	Circuit Tech
Bob Glorioso	MRO1-2/E47	231-5915	Engrg Group Mgr
John Golenbieski	MRO1-2/E47	231-5931	F Box Design Engr
Bill Grundmann	MRO1-2/E47	231-7531	F Box Design Engr
Paul Guglielmi	MRO1-2/E47	231-6506	Clock & Timing Consultant
John Hackenberg	MRO1-2/E47	231-6106	Circuit Engr
Charlie Hall	MRO1-2/E74	231-6758	Engrg Operations Mgr
Doug Hall	MRO1-2/E47	231-6580	Tech
Bob Haller	MRO1-2/E47	231-7520	Circuit Engr
Rob Hannemann	MLO8-3/T13	223-3349	Thermal Consultant
Dennis Hebert	QI-1/B20	276-7231	Advance Test Technology
Robert Hickcox	MRO1-2/E69	231-6227	Computer Services Mgr
Bill Hilliard	MRO1-2/E47	231-4101	E Box Design Engr
Joe Jasniewski	MRO1-2/E47	231-6305	Electrical Engr
Brian Kalita	MLO8-3/T13	223-2824	Thermal Engr
John Kane	LMO	231-4668	Microproducts Purchasing
Stuart Keir	MRO1-2/E47	231-6736	Principal Engr
John Kelly	MRO1-2/E47	231-5488	Circuit Component Supv
Herb Kempton	MRO1-2/E47	231-4153	Emulator Tech
Tom Knight	MRO1-2/E47	231-6112	I Box Design Engr
Alan Kotok	MRO1-2/E47	231-7381	CPU Engrg Mgr
Vic Ku	MRO1-2/E47	231-6202	VENUS Technology Mgr
Jim Lacy	MRO1-2/E47	231-6867	E Box Design Engr
Pete Lawrence	MRO1-2/E47	231-6621	Circuit Packaging Supv
Janice LeBlanc	MRO1-2/E47	231-6460	Administrative Secretary
Dennis Litwinetz	MRO1-2/E47	231-6422	Circuit Engr
Clem Liu	MRO1-2/E47	231-5824	I Box Project Engr
David Low	MLO3-4/T35	223-3694	D-LASAR Engr
Brian Lupaczyk	MRO1-2/E47	231-5564	Project Tech
Craig Maiman	MRO1-2/E47	231-6839	I Box Engr
John Manton	MRO1-2/E47	231-5572	M Box Design Engr
John Martin	MRO1-2/E47	231-6820	M Box Tech
Jim McElroy	MRO1-2/E47	231-6286	Power & Packaging Mgr
Dennis Najarian	MRO1-2/E47	231-6790	Engr
Matt Nolan	MRO1-2/E18	231-6364	Engrg Support Services
Fernando Colon Osorio	MRO1-2/E47	231-7230	Alternative I Box Proj Ldr
Cal Page	MRO1-2/E47	231-2505	Microcode Engr
Ed Papsis	MRO1-2/E47	231-6243	FCC & Internatnl Regs Engr
John Pare	MLO21-2/E64	223-3795	Memory Design Engr
Yale Patt	MRO1-2/E47	231-4187	Consultant
Warren Peluso	MRO1-2/E47	231-5081	Circuit Mgr
Rod Poquadeck	MRO1-2/E47	231-4451	Project Tech
Paul Porreca	MRO1-2/E47	231-6547	Mechanical Engr
Peter Rado	MRO1-2/E47	231-5847	I Box Design Engr
Norbert Riegelhaupt	MLO21-1/E64	223-7689	Memory Storage Array Engr
Eileen Samberg	MRO1-2/E47	231-5014	Microprogrammer

Bob Sanzone	MRO1-2/E47	231-6155	IO Engr
Roger Scott	MRO1-2/E47	231-5136	Mechanical Tech
Ron Setera	MRO1-2/E18	231-6213	Peripherals Group Mgr
Don Simon	LMO2	238-3456	MCA Technical Director, A&T
Bill Smith	MRO1-2/E47	231-4381	Consulting Engr
Kerry Smith	MRO1-2/E47	231-7375	Evaluation Engr
Dan Stirling	MRO1-2/E47	231-4153	Tech
Diane Tinsley	MRO1-2/E47	231-4028	Secretary
Paul Tourigny	MRO1-2/E47	231-5392	Tech
Anh Tran	MRO1-2/E47	231-7232	Circuit Engr
Mario Troiani	MRO1-2/E47	231-6136	Senior Engr
Ken Waine	MRO1-2/E47	231-7523	IO Mgr
Bill Walton	MRO1-2/E47	231-6274	Advanced Devel Engrg Mgr
Jack Ward	MRO1-2/E47	231-6527	E Box Tech
Bruce Weaver	MRO1-2/E47	231-7286	Mechanical Supv
Steve Weston	MRO1-2/E47	231-6833	Mechanical Tech
Jackie Wilson	MRO1-2/E69	231-4081	Computer Services Sys Planner
Albert Yu	MRO1-2/E47	231-5738	I Box Design Engr
Joe Zeh	MRO1-2/G6	231-5924	Technology Mgr
Sultan Zia	MRO1-2/E47	231-6277	Program Mgr

Diagnostics (LVD)

Rachelle Aubut	MRO1-2/E68	231-6439	Diagnostic Engr
Don Ball	MRO1-2/E68	231-6368	M Box Diagnostic Engr
Dick Beaven	MRO1-2/E68	231-6505	LVD Consultant
Dale Cook	MRO1-2/E68	231-6193	Diag Arch & M Box/SBIA Ldr
Bill Dale	MRO1-2/E68	231-6192	Coverage Simulation
Bill Fairing	MRO1-2/E68	231-4057	Microdiagnostic Engr
Helena Flanagan	MRO1-2/E47	231-4030	Secretary
Jim Gallagher	MRO1-2/E47	231-7772	SW Engr (Console)
Carl Gibson	MRO1-2/E78	231-6779	LVD Mgr
Joe Gilby	MRO1-2/E68	231-5800	I Box Diagnostic Engr
Rich Glackemeyer	MRO1-2/E68	231-4083	I Box Diagnostic Engr
Paul Leveille	MRO1-2/E47	231-7753	Diagnostic Engr (Console)
Tom Moore	MRO1-2/E68	231-4038	SBIA Diagnostic Engr
Bob Petty	MRO1-2/E68	231-5102	Diag Ldr (Console, Processor)
Mark Roch	MRO1-2/E68	231-6755	EMM Firmware Engr
Milton Shively	MRO1-2/E68	231-6317	F Box Diagnostic Engr
Bob Somers	MRO1-2/E47	231-4215	Diagnostic Consultant
Jack Stansbury	TWO/F18	247-2846	Diagnostic Supv Maintainer
George Stevens	MRO1-2/E68	231-6750	SW Engr (Console)
Dave Tibbetts	MRO1-2/E68	231-6268	E Box Diagnostic Engr

Software Engineering

Norma Abel	ZKO1-3/D40	264-8138	Technical Languages
John Anderson	MKO1-2/D03	264-7783	Commercial SW Engrg
Joe Carchidi	ZKO1-1/D42	264-8426	VMS Development Mgr
Wayne Cardoza	ZKO1-1/D42	264-8600	VMS Developer
John Ciukaj	TWO/F18	247-2218	Diagnostic Tools
Ron Criss	MRO1-2/L08	231-5243	1020 SW Engrg Mgr
Geoff Feldman	MRO1-2/E78	231-6259	SW Integration Project Ldr

Kurt Friedrich	ZKO1-3/J33	264-8328	BSSG Product Management
Dick Hustvedt	ZKO1-1/D42	264-8397	VMS Architect
Trevor Kempsell	ZKO1-3/J33	264-8325	VMS Product Mgr
Nancy Kronenberg	ZKO1-1/D42	264-8455	VMS Supv
Trudy Matthews	ZKO1-1/D42	264-8406	VMS Project Ldr
Trev Porter	ZKO1-1/D42	264-8449	VMS Release 3 Project Ldr
Benn Schreiber	ZKO1-2/D42	264-8450	VMS Developer
Armando Stettner	MKO1-1/D29	264-5485	Senior SW Engr

Customer Services

Gary Blenis	MRO1-1/S35	231-4425	Maintainability Engrg Mgr
Jurgen Brommelhoff	MRO1-1/S35	231-4778	Maintainability Engrg Mgr
Reg Burgess	MRO1-1/S35	231-4484	Maintainability Engrg Mgr
Darwin Hatheway	MRO1-1/S35	231-7585	Maintainability Engr
Carl Johnson	MRO1-1/S35	231-4452	Project Specialist
Kevin Lynch	MRO1-1/S35	231-4746	Software Services
Walter Manter	MRO1-1/S35	231-6503	Maintainability Engrg Mgr
Art O'Donnell	MRO1-1/S35	231-6231	Maintainability Mgr
Andy Oppenheim	MRO1-1/S35	231-4238	Maintainability Engr
Cal Overhulser	OGO1-2/F11	276-9787	SSG Product Mgr
Frank Robbins	MRO1-1/S35	231-4479	Maintainability Engr
Ron Rocheleau	MRO1-2/S35	231-5147	Maintainability Engr
Jack Walden	MRO1-1/S35	231-5125	SW Services Mgr

Manufacturing

George Beckner	LJO/B2	282-2103	PCB & Module Assembly
John Belanger	APO	280-7213	MSL Program Mgr
Walt Bilosz	LJO/B1	282-2139	Senior Producibility Engr
Marie Blocker	MRO1-3/P78	231-6692	Integration Mfg Engr
Howard Carter	MRO1-3/P25	231-5686	Mfg Engrg Sys Test Engr
Dick Cygan	MRO1-3/P25	231-5123	Mfg New Products Qual Engr
Ray DelGuidice	MRO1-3/B41	231-5251	Mfg Engr
Ted Eck	QI-2/C21	223-4596	MTP Testability Engr
Pete Emery	MRO1-2/M53	231-4401	MEC Mgr
John Ewalt	MRO1-2/M53	231-7590	Planning and Schedule Mgr
Dave Fisher	MRO1-3/P25	231-5662	Mfg Engrg SW Mgr
Jim Foran	MRO1-3/P78	231-5970	Purchased Material Qual Mgr
Whitey Gibeault	MRO1-2/M53	231-6065	New Products Mechanical Engr
John Grose	MRO1-2/M53	231-5265	Mfg Project Mgr
Tom Hagspiel	MRO1-3/P78	231-6186	Mfg Engrg Process Mgr
Linda Hart	MRO1-2/M53	231-5420	Overall Planner
Vickie Hayes	ACO/E44	232-2503	Mfg New Products Planner
Jim Eden-Kilgour	ACO/E44	232-2371	Sr Mfg Engr
Van Krikorian	MRO1-3/P25	231-7634	Qual Assurance Mgr
Bob Latvalla	MRO1-3/P76	231-5558	Reliability Mgr
Bill Lord	MRO1-3/P78	231-6339	Sr Module Assy Engr
Jeff Mariano	MRO1-3/P25	231-6054	Sys Mfg Engrg Mgr
Bill Martel	MRO1-2/M53	231-6467	Sys Mfg Program Mgr
John McCaffery	MRO1-3/P78	231-6240	Sr Cable & Harness Assy Engr
John Mitchell	MRO1-3/P25	231-4858	Mfg Interconnect Proj Mgr

Steve Moro	MRO1-3/P78	231-5667	Mfg Engrg Module Test Engr
Bob Murphy	MRO1-2/M53	231-5244	Sys Mfg Program Mgr
Jack Parker	MRO1-3/P78	231-4503	CPU Cab Assy Engr
Bharat Patel	ACO/B73	232-2236	Mfg Test Applications Mgr
David Ragwar	MRO1-3/P76	231-4934	Reliability Engr
Don Reczek	MRO1-3/P25	231-6483	Mfg Engrg Test Mgr
Bob Reed	MRO1-3/P78	231-6393	Mfg Engrg Test Supv
Bob Ridley	MRO1-3/P78	231-6034	Sr Packaging Engr
Moshe Roditi	MRO1-3/P25	231-4827	Mfg Integration Mgr
Bill Saltys	ACO/S20	232-2499	Computer Sys Adv Process Mgmt
Jim Scanlan	MRO1-3/P78	231-5663	Mfg Engrg Test Strategist
John Shea	MRO1-2/E47	231-5960	Pincut Tech
Laura Startzenbach	MRO1-3/P25	231-4559	Mfg Engrg Sys Test Engr
Graham Swift	MRO1-3/P78	231-7271	Mfg Project Ldr
Jack Zorabedian	MRO1-3/P78	231-6095	Assembly Engrg Mgr

Educational Services D & P

Rich Candor	MRO1-2/T17	231-5011	ESDP Unit Mgr
Art Johnson	MRO1-2/E17	231-6250	Technical Writer
Larry Mello	MRO1-2/E17	231-4018	Hardware Course Developer
Ken Robinson	BUO/E38	249-4722	VAX Group Unit Mgr
Manny Simonian	MRO1-2/E17	231-5287	Technical Writer
Bob Skillen	BUO/E41	249-4714	Training Operations

Architecture

Dileep Bhandarkar	TWO/B05	247-2041	VAX Architecture Mgr

RAMP Engineering

John Shebell	PKO3-2/S53	223-3101	Corporate RAMP Engrg

Educational Marketing

Rick Grady	MRO2-2/8D2	231-4436	LCG Marketing Specialist
Frans van der Molen	MRO1-1/M89	231-5984	Marketing Analyst

Performance Analysis

Karen Dorhamer	HLO2-3/C09	225-5947	Performance Analyst
Bhagyam Moses	MLO3-3/H24	223-7909	Performance Analyst
Steve Neupauer	MR01-2/G6	231-7754	Performance Analyst

CAD Support

Jerry Bixby	MRO1-2/E74	231-6781	SUDS Tech
Tom Bowen	MRO1-2/E74	231-6995	SUDS Supv
Lisa Chaves	MRO1-2/E74	231-6215	SUDS Tech
Roger Pothier	MRO1-2/E74	231-6710	Engrg Services Mgr
Dotti Rado	MRO1-2/E74	231-6650	PC and IC Mgr
Pat Shoreman	MRO1-2/E74	231-6573	SUDS Tech
Dave Sireen	MRO1-2/E74	231-6712	Drafting Supv
Lorrie Wu	MRO1-2/E74	231-6781	Multiwire Designer

LSCAD Development

Gary Brown	MRO1-2/E89	231-7499	Simulation
Joe Bruen	MRO1-2/E89	231-4898	Delay Analysis
Steve Ching	MRO1-2/E89	231-4053	TUMS Simulation Project Ldr
Mike Cowperthwaite	MRO1-2/E89	231-7297	Jr Co-op Engr
Dave DeCenzo	MRO1-2/E89	231-6230	CAD Programmer
Ted Elkind	MRO1-2/E89	231-6828	Delay Analysis Project Ldr
Tim Fennell	MRO1-2/E89	231-7291	SW Engr
Jim Klinkenberg	MRO1-2/E89	231-4087	IDEA Engr
Don Langbein	MRO1-2/E89	231-5458	Consultant
Paul Lucier	MRO1-2/E89	231-7223	TUMS Simulation Engr
John McAllen	MRO1-2/E89	231-4782	TUMS Simulation Engr
Mike Newman	MRO1-2/E89	231-5007	CAD Programmer
Dan O'Brien	MRO1-2/E89	231-5099	Senior SW Engr
George Rogers	MRO1-2/E89	231-5458	Senior Engr
Steve Root	MRO1-2/E89	231-4456	FINCUT Engr
Jeff Singer	MRO1-2/E78	231-4650	CAD-CAM Mgr
Chuck Smith	MRO1-2/E89	231-6754	Operations Analyst
Vehbi Tasar	MRO1-2/E89	231-5565	LSCAD Mgr
Keith Yesse	MRO1-2/E89	231-6984	Senior SW Engr

GLOSSARY

Product Announcement
: The point in time when we formally announce to the public details regarding the product and its availability.

First Revenue Ship (FRS)
: This is an Engineering goal. It is the date when we plan to ship the first unit from FA&T to a paying external customer. This used to be referred to as "First Customer Ship" (FCS).

First Volume Commit (FVC)
: The date when Volume Manufacturing plans to make its first production shipment to FA&T. This plan is confirmed in the Request/Commit System.

First Volume Ship (FVS)
: The actual date that Volume Manufacturing ships the first production unit to FA&T. Thus this even is a measure of FVC achievement, and it is confirmed in the Delivery Report system.

Product Availability (PA)
: The date when we plan to have product line inventories available. This is also the first period for which revenue (ship) forecasts can be submitted. PA is assumed to be six months after FVC until Product announcement, at which time PA becomes firm.

ALU	Arithmetic and logical unit
BMC	Basic monthly charge
CAD	Computer aided design
CI	Computer interconnect
CIA	CI adapter
CIS	Commercial instruction set
CPA	CI port adapter
CSA	Canadian Standards Association
DBMS	Database management system
DDC	Digital Diagnosis Center
DMT	Design maturity test
DVT	Design verification test
ECL	Emitter-coupled logic
FCS	First customer ship (now FRS)
FRS	First revenue ship
FVC	First volume commit
FRU	Field replacement unit
FVS	First volume ship
HPP	Heat pin planar

HSC	Hierarchical storage controller
IATF	Interconnect Architecture Task Force
IEC	International Electrotechnical Commission
IQ	Index of Quality
LCC	Life cycle cost
LSI	Large scale integration
MBA	Massbus adapter
MCA	Macrocell array
MDT	Mean down time
MEG	Maintainability Engineering Group
MSL	Multi-signal layer (controlled impedance)
MTF	Marketing Task Force
MU	Markup
NI	Network interconnect
NMOS	Negative MOS
NPA	NI Port Adapter
OOD	Office of Operations and Development
PA	Product availability
PCM	Plug compatible manufacturer
PMT	Process maturity test
QA	Quality assurance
QBON	Quick verify, bed-of-nails
QV	Quality verification
RAMP	Reliability Availability Maintainability Program
RD	Remote diagnosis
SAGE	Simulation of asynchronous gate elements
SBI	Synchronous backplane interconnect
SBIA	SBI adapter
SDC	Software Distribution Center
SDI	Standard disk interface
SI	Storage interconnect
SMP	Symmetrical multiprocessing
SMT	System maturity test
SPR	Software problem report
STI	Standard tape interface
TTL	Transistor-transitor logic
UBA	Unibus adapter
UDA	Unibus disk adapter
UETP	User environmental test package
VOTE	Verification of test effectiveness
X25	European communication protocol standard